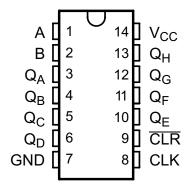


## 8-Bit Parallel-Out Serial Shift Registers

Check for Samples: SN54HC164, SN74HC164

#### **FEATURES**

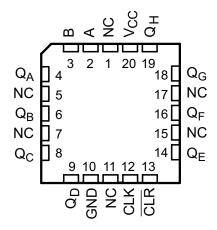
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80-μA Max I<sub>CC</sub>
- Typical t<sub>pd</sub>= 20 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1-μA Max
- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear



SN54HC164...J OR W PACKAGE SN74HC164...D, N, NS, OR PW PACKAGE (TOP VIEW)

### DESCRIPTION

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear (CLR) input. The gated serial (A and B) inputs permit complete control over incoming data; a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock (CLK) pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while CLK is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of CLK.



NC - No internal connection

SN54HC164...FK PACKAGE (TOP VIEW)

#### **FUNCTION TABLE**<sup>(1)(2)</sup>

	INP	UTS			OUTPU	JTS	
CLR	CLK	Α	В	$Q_A$	$Q_{B}$		$Q_{H}$
L	Χ	Χ	Χ	L	L		L
Н	L	Χ	Χ	$Q_{A0}$	$Q_{B0}$		$Q_{H0}$
Н	<b>↑</b>	Н	Н	Н	$Q_An$		$Q_{Gn}$
Н	<b>↑</b>	L	X	L	$Q_An$		$Q_{Gn}$
Н	1	Χ	L	L	$Q_An$		$Q_{Gn}$

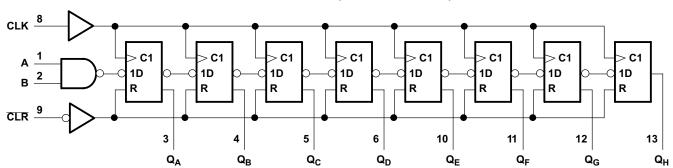
- Q<sub>A0</sub>, Q<sub>B0</sub>, Q<sub>H0</sub> = the level of Q<sub>A</sub>, Q<sub>B</sub>, or Q<sub>H</sub>, respectively, before the indicated steady-state input conditions were established.
- (2) Q<sub>An</sub>, Q<sub>Gn</sub> = the level of Q<sub>A</sub> or Q<sub>G</sub> before the most recent ↑ transition of CLK: indicates a 1-bit shift.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

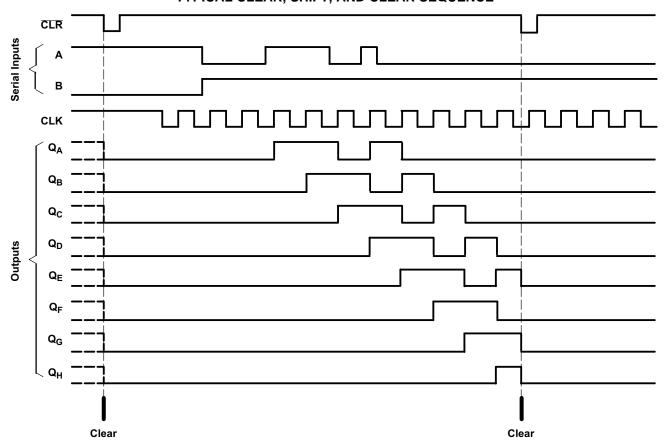


### LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the D, J, N, NS, PW, and W packages.

### TYPICAL CLEAR, SHIFT, AND CLEAR SEQUENCE





#### **ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNITS
V <sub>CC</sub>	Supply voltage range		-0.5	7	V
I <sub>IK</sub>	Input clamp current	$V_{I} < 0 \text{ or } V_{I} > V_{CC}^{(2)}$		±20	mA
I <sub>OK</sub>	Output clamp current	$V_1 < 0 \text{ or } V_1 > V_{CC}^{(2)}$ $V_0 < 0 \text{ or } V_0 > V_{CC}^{(2)}$		±20	mA
Io	Continuous output current	$V_O = 0$ to $V_{CC}$		±25	mA
	Continuous current through V <sub>CC</sub> or G		±50	mA	
		D package		86	
$\theta_{JA}^{(3)}$	Declare the week income done	N package		80	90/14/
OJA (°)	Package thermal impedance	NS package		76	°C/W
		PW package		113	
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS(1)

			SN	54HC164		SI	N74HC164		LINUT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2	5	6	2	5	6	V
		V <sub>CC</sub> = 2 V	1.5			1.5			
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 4.5 V	3.15			3.15			V
		V <sub>CC</sub> = 6 V	4.2			4.2			
		V <sub>CC</sub> = 2 V			0.5			0.5	
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 4.5 V			1.35			1.35	V
		V <sub>CC</sub> = 6 V			1.8			1.8	
VI	Input voltage		0		V <sub>CC</sub>	0		V <sub>CC</sub>	V
Vo	Output voltage		0		V <sub>CC</sub>	0		V <sub>CC</sub>	V
		V <sub>CC</sub> = 2 V			1000			1000	
$\Delta t/\Delta v^{(2)}$	Input transition rise/fall time	V <sub>CC</sub> = 4.5 V			500			500	ns
		V <sub>CC</sub> = 6 V			400			400	
T <sub>A</sub>	Operating free-air temperature	•	-55		125	-40		125	°C

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

Product Folder Links: SN54HC164 SN74HC164

<sup>(2)</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>(3)</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

<sup>(2)</sup> If this device is used in the threshold region (from V<sub>IL</sub> max = 0.5 V to V<sub>IH</sub> min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t<sub>t</sub> = 1000 ns and V<sub>CC</sub> = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.



#### **ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>cc</sub>	V <sub>CC</sub>			SN54H –55°C to		SN74HC164 -55°C to 85°C		Recomm SN74H0 –55°C to	UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	$V_I = V_{IH}$ or $V_{IL}$	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9		1.9		1.9		
			4.5 V	4.4	4.499		4.4		4.4		4.4		
$V_{OH}$			6 V	5.9	5.999		5.9		5.9		5.9		V
		I <sub>OH</sub> = −4 mA	4.5 V	3.98	4.3		3.7		3.84		3.7		
		I <sub>OH</sub> = −5.2 mA	6 V	5.48	5.8		5.2		5.34		5.2		
		I <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1		0.1		0.1	
			4.5 V		0.001	0.1		0.1		0.1		0.1	
$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$		6 V		0.001	0.1		0.1		0.1		0.1	V
		I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26		0.4		0.33		0.4	
		I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26		0.4		0.33		0.4	
I <sub>I</sub>	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000		±1000	nA
I <sub>CC</sub>	$V_I = V_{CC}$ or 0	I <sub>O</sub> = 0	6 V			8		160		80		160	μΑ
C <sub>i</sub>			2 V to 6 V		3	10		10		10		10	pF

### **TIMING REQUIREMENTS**

over recommended operating free-air temperature range (unless otherwise noted)

	PARAN	IETER	V <sub>cc</sub>	T <sub>A</sub> = 25	T <sub>A</sub> = 25°C		SN54HC164 -55°C to 125°C		C164 85°C	Recomm SN74H0 –55°C to	C164	UNIT
		MIN MAX MIN MAX MI						MIN	MAX	MIN	MAX	
			2 V		6		4.2		5		4.2	
f <sub>clock</sub>	Clock frequen	су	4.5 V		31		21		25		21	MHz
			6 V		36		25		28		25	
			2 V	100		150		125		125		
		CLR low	4.5 V	20		30		25		25	-	
	Pulse		6 V	17		25		21		21		ns
t <sub>w</sub>	duration		2 V	80		120		100		120		ns
		CLK high or low	4.5 V	16		24		20		24		
			6 V	14		20		18		20		
			2 V	100		150		125		125		
		Data	4.5 V	20		30		25		25		
	Setup time		6 V	17		25		21		25		nc
t <sub>su</sub>	before CLK↑		2 V	100		150		125		125		ns
		CLR inactive	4.5 V	20		30		25		25		
			6 V	17		25		21		25		
				5		5		5		5		
t <sub>h</sub>	Hold time, data	Hold time, data after CLK↑	4.5 V	5		5		5		5		ns
			6 V	5		5		5		5		

Product Folder Links: SN54HC164 SN74HC164

Submit Documentation Feedback

Copyright © 1982–2013, Texas Instruments Incorporated



#### **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range, C<sub>1</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETE R	FROM (INPUT)	TO (OUTPUT	V <sub>cc</sub>	TA	= 25°C		SN54H0 -55°C to		SN74H0 –55°C to		Recomme SN74HC –55°C to 1	164	UNIT
	, ,	,		MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
			2 V	6	10		4.2		5		42		
$f_{\text{max}}$			4.5 V	31	54		21		25		21		MHz
			6 V	36	62		25		28		25		
			2 V		140	205		295		255		255	
t <sub>PHL</sub>	CLR	Any Q	4.5 V		28	41		59		51		51	
			6 V		24	35		51		46		46	
			2 V		115	175		265		220		220	ns
$t_{pd}$	CLK	Any Q	4.5 V		23	35		53		44		44	
			6 V		20	30		45		38		38	
			2 V		38	75		110		95		110	
t <sub>t</sub>			4.5 V		8	15		22		19		22	ns
			6 V		6	13		19		16		19	

### **OPERATING CHARACTERISTICS**

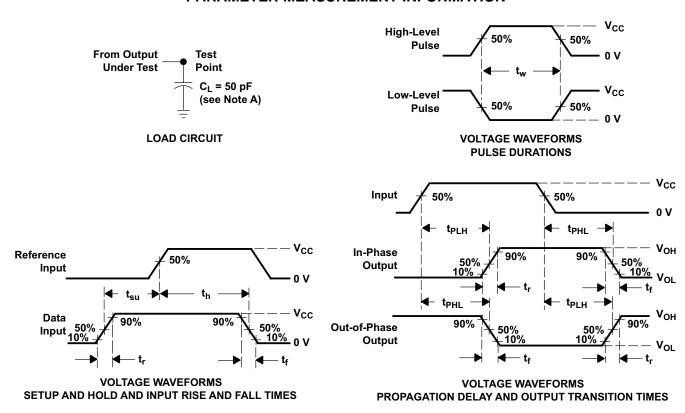
 $T_A = 25^{\circ}C$ 

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load	135	pF

Product Folder Links: SN54HC164 SN74HC164



#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> = 6 ns, t<sub>f</sub> = 6 ns.
  - C. For clock inputs,  $f_{\text{max}}$  is measured when the input duty cycle is 50%.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

Submit Documentation Feedback



### **REVISION HISTORY**

CI	Changes from Revision E (November 2010) to Revision F								
•	Updated document to new TI data sheet format - no specification changes.	1							
•	Removed ordering information.	1							
•	Updated operating temperature range.	3							

Product Folder Links: SN54HC164 SN74HC164





4-Dec-2014

### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Sample
5962-8416201VCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8416201VC A SNV54HC164J	Sample
5962-8416201VDA	ACTIVE	CFP	W	14	25	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8416201VD A SNV54HC164W	Sample
84162012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84162012A SNJ54HC 164FK	Sample
8416201CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8416201CA SNJ54HC164J	Sample
SN54HC164J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54HC164J	Sample
SN74HC164D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	Sample
SN74HC164DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	Sampl
SN74HC164DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	Sampl
SN74HC164DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	HC164	Sampl
SN74HC164DRG3	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	HC164	Sampl
SN74HC164DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	Sampl
SN74HC164DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	Sampl
SN74HC164N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU   CU SN	N / A for Pkg Type	-40 to 125	SN74HC164N	Sampl
SN74HC164N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	-40 to 125		
SN74HC164NE3	PREVIEW	PDIP	N	14	25	TBD	Call TI	Call TI	-40 to 125	SN74HC164N	
SN74HC164NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	SN74HC164N	Sampl
SN74HC164NSR	ACTIVE	so	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	Samp



### PACKAGE OPTION ADDENDUM

4-Dec-2014

Orderable Device	Status	Package Type		Pins		Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
SN74HC164PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	Samples
SN74HC164PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	Samples
SN74HC164PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	HC164	Samples
SN74HC164PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	Samples
SN74HC164PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	Samples
SN74HC164PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	Samples
SN74HC164PWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC164	Samples
SNJ54HC164FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84162012A SNJ54HC 164FK	Samples
SNJ54HC164J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8416201CA SNJ54HC164J	Samples
SNJ54HC164W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8416201DA SNJ54HC164W	Samples

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

### PACKAGE OPTION ADDENDUM



4-Dec-2014

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN54HC164, SN54HC164-SP, SN74HC164:

Catalog: SN74HC164, SN54HC164

Military: SN54HC164

7110-1110-10-1

Space: SN54HC164-SP

NOTE: Qualified Version Definitions:

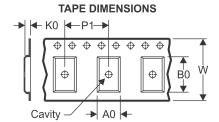
- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application

### PACKAGE MATERIALS INFORMATION

www.ti.com 7-Apr-2014

### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC164DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC164DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC164DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
SN74HC164DRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
SN74HC164DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC164DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC164DT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC164NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC164PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC164PWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

www.ti.com 7-Apr-2014



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC164DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC164DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC164DR	SOIC	D	14	2500	364.0	364.0	27.0
SN74HC164DRG3	SOIC	D	14	2500	364.0	364.0	27.0
SN74HC164DRG4	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC164DRG4	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC164DT	SOIC	D	14	250	367.0	367.0	38.0
SN74HC164NSR	SO	NS	14	2000	367.0	367.0	38.0
SN74HC164PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HC164PWT	TSSOP	PW	14	250	367.0	367.0	35.0

### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## W (R-GDFP-F14)

### CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14



## FK (S-CQCC-N\*\*)

### LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



### N (R-PDIP-T\*\*)

### PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



### D (R-PDSO-G14)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



# D (R-PDSO-G14)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
  - Sody length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



## PW (R-PDSO-G14)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



### **MECHANICAL DATA**

### NS (R-PDSO-G\*\*)

## 14-PINS SHOWN

### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



#### IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have not been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

#### **Products Applications**

logic.ti.com

Audio www.ti.com/audio Automotive and Transportation www.ti.com/automotive **Amplifiers** amplifier.ti.com Communications and Telecom www.ti.com/communications **Data Converters** dataconverter.ti.com Computers and Peripherals www.ti.com/computers **DLP® Products** www.dlp.com Consumer Electronics www.ti.com/consumer-apps DSP dsp.ti.com **Energy and Lighting** www.ti.com/energy Clocks and Timers www.ti.com/clocks Industrial www.ti.com/industrial Interface interface.ti.com Medical www.ti.com/medical Logic Security www.ti.com/security

Power Mgmt Space, Avionics and Defense www.ti.com/space-avionics-defense power.ti.com

Microcontrollers www.ti.com/video microcontroller.ti.com Video and Imaging

www.ti-rfid.com

**OMAP Applications Processors TI E2E Community** www.ti.com/omap e2e.ti.com

Wireless Connectivity www.ti.com/wirelessconnectivity