

NC7SZ18

TinyLogic UHS 1-of-2 Non-Inverting De-multiplexer with 3-STATE Deselected Output

Description

The NC7SZ18 is a 1-of-2 non-inverting demultiplexer. The device will buffer the data on the A pin and pass to either output Y_0 or Y_1 dependent on whether state of the select pin (S) is LOW or HIGH respectively. The deselected output will be placed into a high impedance state. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over the 1.65 V to 5.5 V V_{CC} operating range. The inputs and outputs are high impedance when V_{CC} is 0 V. Inputs tolerate voltages up to 5.5 V independent of V_{CC} operating range.

Features

- Ultra High-Speed: t_{PD} 2.5 ns Typical at 5 V V_{CC}
- High Impedance Output when Deselected
- Broad V_{CC} Operating Range: 1.65 V to 5.50 V
- Power Down High Impedance Inputs / Outputs
- Over-Voltage Tolerance Inputs Facilitate 5 V to 3 V Translation
- Proprietary Noise / EMI Reduction Circuitry
- Ultra-Small MicroPak™ Packages
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



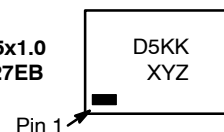
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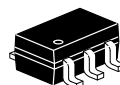
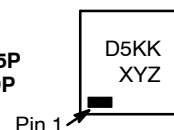
MARKING DIAGRAMS



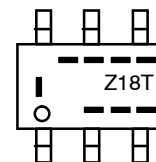
SIP6 1.45x1.0
CASE 127EB



UDFN6
1.0X1.0, 0.35P
CASE 517DP



SC-88
(SC-70 6 Lead)
1.25x2
CASE 419AD-01



D5, Z18 = Specific Device Code
KK = 2-Digit Lot Run Traceability Code
XY = 2-Digit Date Code Format
Z = Assembly Plant Code
---- = Year Coding Scheme
|•-- = Plant Code Identifier
T = Die Run Code
--- = Eight-Week Datacoding Scheme

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

NC7SZ18

Pin Configurations

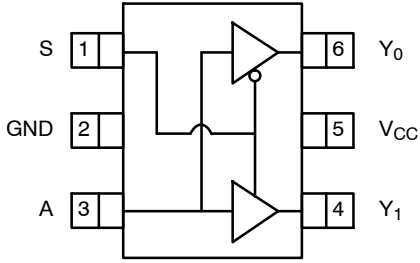


Figure 1. SC70 (Top View)

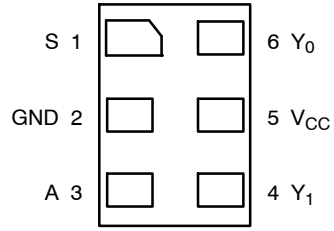
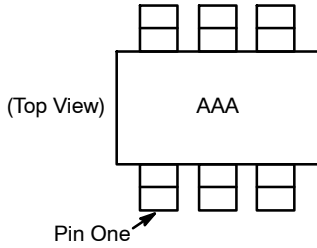


Figure 2. MicroPak (Top Through View)



NOTES:

1. AAA represents product code top mark (see [Ordering Information](#)).
2. Orientation of top mark determines pin one location.
3. Reading the top mark left to right, pin one is the lower left pin.

Figure 3. Pin 1 Orientation

PIN DEFINITIONS

Pin # SC70	Pin # MicroPak	Name	Description
1	1	S	Data Input
2	2	GND	Ground
3	3	A	Demultiplexer Data
4	4	Y ₁	Output
5	5	V _{CC}	Supply Voltage
6	6	Y ₀	Output

FUNCTION TABLE

Inputs		Output	
S	A	Y ₀	Y ₁
L	L	L	Z
L	H	H	Z
H	L	Z	L
H	H	Z	H

H = HIGH Logic Level
 L = LOW Logic Level
 X = 3-STATE

NC7SZ18

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V _{CC}	Supply Voltage		-0.5	6.5	V
V _{IN}	DC Input Voltage		-0.5	6.5	V
V _{OUT}	DC Output Voltage		-0.5	6.5	V
I _{IK}	DC Input Diode Current	V _{IN} ≤ -0.5 V	-	-50	mA
I _{OK}	DC Output Diode Current	V _{OUT} ≤ -0.5 V	-	-50	mA
I _{OUT}	DC Output Current		-	±50	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current		-	±100	mA
T _{STG}	Storage Temperature Range		-65	+150	°C
T _J	Junction Temperature Under Bias		-	+150	°C
T _L	Junction Lead Temperature (Soldering, 10 Seconds)		-	+260	°C
P _D	Power Dissipation at +85°C	SC70-6	-	190	mW
		MicroPak-6	-	327	
		MicroPak2™-6	-	327	
ESD	Human Body Model, JEDEC: JESD22-A114		-	4000	V
	Charge Device Model, JEDEC: JESD22-C101		-	2000	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply Voltage Operating		1.65	5.50	V
	Supply Voltage Data Retention		1.5	5.5	
V _{IN}	Input Voltage		0	5.5	V
V _{OUT}	Output Voltage		0	V _{CC}	V
t _r , t _f	Input Rise and Fall Times	V _{CC} at 1.8 V ±0.15 V, 2.5 V ±0.2 V	0	20	ns/V
		V _{CC} at 3.3 V ±0.3 V	0	10	
		V _{CC} at 5.0 V ±0.5 V	0	5	
T _A	Operating Temperature		-40	+85	°C
θ _{JA}	Thermal Resistance	SC70-6	-	659	°C/W
		MicroPak-6	-	382	
		MicroPak2-6	-	382	°C/W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NC7SZ18

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C			T _A = -40 to +85°C		Unit	
				Min	Typ	Max	Min	Max		
V _{IH}	HIGH Level Input Voltage	1.65 to 1.95		0.65 V _{CC}	-	-	0.75 V _{CC}	-	V	
		2.30 to 5.50		0.70 V _{CC}	-	-	0.70 V _{CC}	-		
V _{IL}	LOW Level Input Voltage	1.65 to 1.95		-	-	0.25 V _{CC}	-	0.25 V _{CC}	V	
		2.30 to 5.50		-	-	0.30 V _{CC}	-	0.30 V _{CC}		
V _{OH}	HIGH Level Output Voltage	1.65	V _{IN} = V _{IH} , I _{OH} = -100 μA	1.55	1.65	-	1.55	-	V	
		2.30		2.20	2.30	-	2.20	-		
		3.00		2.90	3.00	-	2.90	-		
		4.50		4.40	4.50	-	4.40	-		
		1.65	I _{OH} = -4 mA	1.29	1.52	-	1.29	-		
		2.30		I _{OH} = -8 mA	1.90	2.15	-	1.90		-
		3.00		I _{OH} = -16 mA	2.40	2.80	-	2.40		-
		3.00		I _{OH} = -24 mA	2.30	3.68	-	2.30		-
		4.50		I _{OH} = -32 mA	3.80	4.20	-	3.80		-
V _{OL}	LOW Level Output Voltage	1.65	V _{IN} = V _{IL} , I _{OL} = 100 μA	-	0.00	0.10	-	0.10	V	
		2.30		-	0.00	0.10	-	0.10		
		3.00		-	0.00	0.10	-	0.10		
		4.50		-	0.00	0.10	-	0.10		
		1.65	I _{OL} = 4 mA	-	0.08	0.24	-	0.24		
		2.30		I _{OL} = 8 mA	-	0.10	0.30	-		0.30
		3.00		I _{OL} = 16 mA	-	0.15	0.40	-		0.40
		3.00		I _{OL} = 24 mA	-	0.22	0.55	-		0.55
		4.50		I _{OL} = 32 mA	-	0.22	0.55	-		0.55
I _{IN}	Input Leakage Current	1.65 to 5.5	V _{IN} = 5.5 V, GND	-	-	±0.1	-	±1.0	μA	
I _{OZ}	3-STATE Output Leakage	1.65 to 5.50	V _{IN} = V _{IL} or V _{OH} , 0 < V _{OUT} ≤ 5.5 V	-	-	±0.5	-	±5.0	μA	
I _{OFF}	Power Off Leakage Current	0	V _{IN} or V _{OUT} = 5.5 V	-	-	1	-	10	μA	
I _{CC}	Quiescent Supply Current	1.65 to 5.50	V _{IN} = 5.5 V, GND	-	-	1	-	10	μA	

NC7SZ18

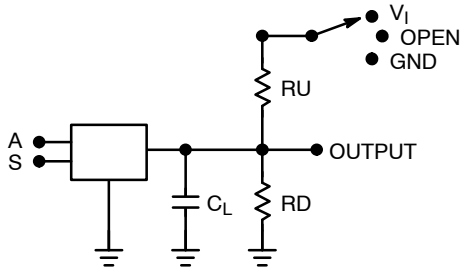
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C			T _A = -40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay A to Y ₀ or Y ₁ (Figure 4, 6)	1.80 ±0.15	C _L = 15 pF, R _D = 1 MΩ, V ₁ = OPEN	-	6.3	10.1	-	10.5	ns
		2.50 ±0.20		-	3.6	5.7	-	6.0	
		3.30 ±0.30		-	2.7	4.0	-	4.3	
		5.00 ±0.50		-	2.0	3.1	-	3.3	
		3.30 ±0.30	C _L = 50 pF, R _D = 500 Ω, V ₁ = OPEN	-	3.4	4.9	-	5.4	ns
		5.00 ±0.50		-	2.5	3.9	-	4.2	
t _{PZL} , t _{PHZ}	Output Enable Time (Figure 4, 6)	1.80 ±0.15	C _L = 50 pF, R _D , R _U = 500 Ω, V ₁ = GND for t _{PHZ} V ₁ = V _{IN} for t _{PZL} V _{IN} = 2 x V _{CC}	-	6.9	12.0	-	12.5	ns
		2.50 ±0.20		-	4.2	6.8	-	7.3	
		3.30 ±0.30		-	3.2	5.0	-	5.5	
		5.00 ±0.50		-	2.5	4.0	-	4.3	
	Output Disable Time (Figure 4, 6)	1.80 ±0.15	C _L = 50 pF, R _D , R _U = 500 Ω, V ₁ = GND for t _{PHZ} V ₁ = V _{IN} for t _{PLZ} V _{IN} = 2 x V _{CC}	-	6.0	10.0	-	10.5	ns
		2.50 ±0.20		-	4.0	6.8	-	7.1	
		3.30 ±0.30		-	2.9	4.9	-	5.3	
		5.00 ±0.50		-	1.8	3.5	-	3.7	
C _{IN}	Input Capacitance	0		-	2.5	-	-	-	pF
C _{OUT}	Output Capacitance	0		-	4.0	-	-	-	pF
C _{PD}	Power Dissipation Capacitance (Note 4) (Figure 5)	3.30		-	16.0	-	-	-	pF
		5.00		-	19.5	-	-	-	

4. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression:
 $I_{CCD} = (C_{PD}) (V_{CC}) (f_{IN}) + (I_{CCstatic})$.

NC7SZ18

AC Loading and Waveforms



- NOTES:
 5. C_L includes load and stray capacitance.
 6. Input PRR = 1.0 MHz, $t_W = 500$ ns.

Figure 4. AC Test Circuit

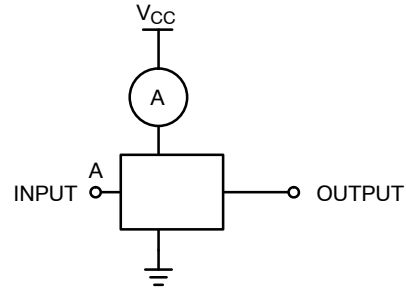


Figure 5. I_{CCD} Test Circuit

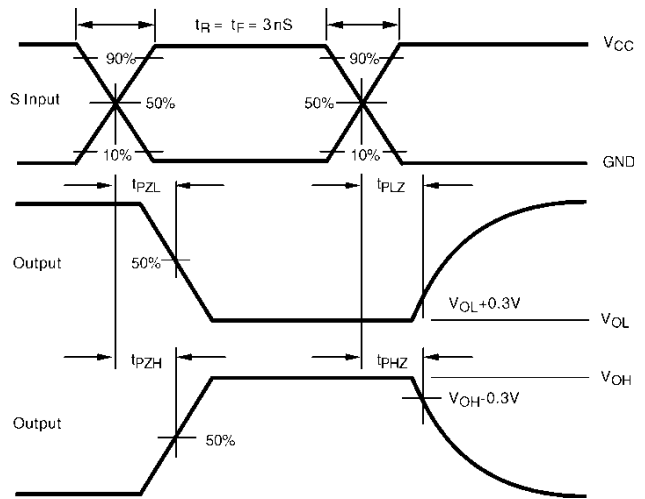
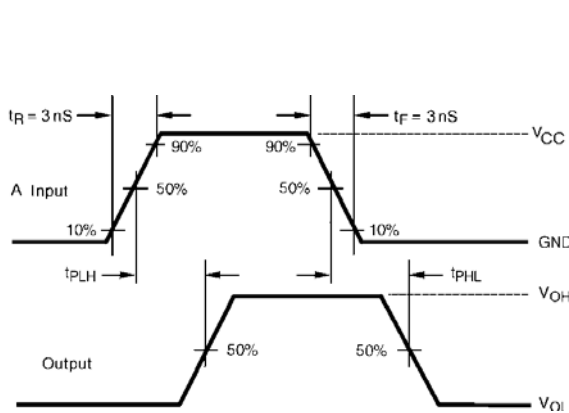


Figure 6. AC Waveforms

ORDERING INFORMATION

Device	Top Mark	Packages	Shipping [†]
NC7SZ18P6X	Z18	6-Lead SC70, EIAJ SC88, 1.25 mm Wide	3000 / Tape & Reel
NC7SZ18L6X	D5	6-Lead MicroPak, 1.00 mm Wide	5000 / Tape & Reel
NC7SZ18FHX	D5	6-Lead, MicroPak2, 1x1 mm Body, .35 mm Pitch	5000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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SIP6 1.45X1.0
CASE 127EB
ISSUE O

DATE 31 AUG 2016



NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

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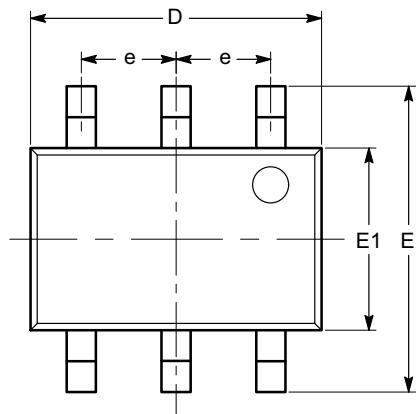
PACKAGE DIMENSIONS

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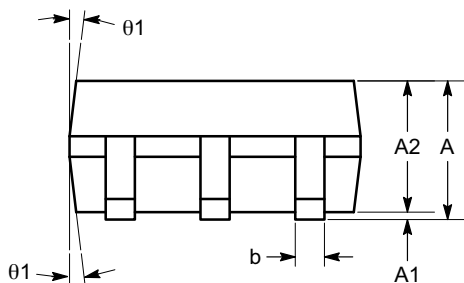
SC-88 (SC-70 6 Lead), 1.25x2
CASE 419AD-01
ISSUE A

DATE 07 JUL 2010

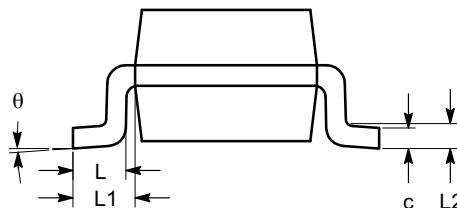


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.26	0.36	0.46
L1	0.42 REF		
L2	0.15 BSC		
θ	0°		8°
θ_1	4°		10°



SIDE VIEW



END VIEW

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-203.

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MECHANICAL CASE OUTLINE

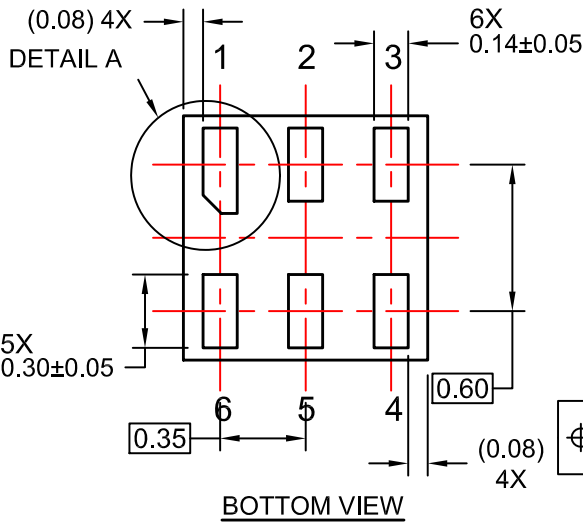
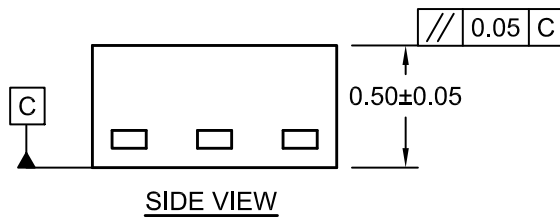
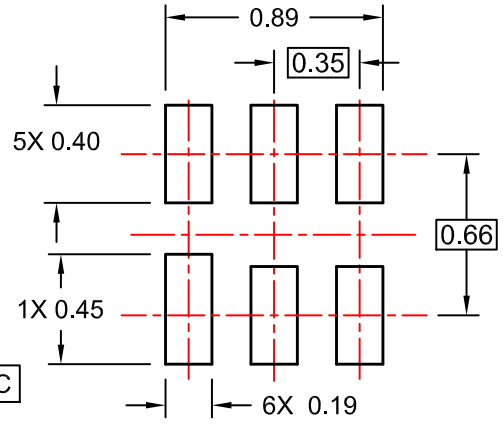
PACKAGE DIMENSIONS

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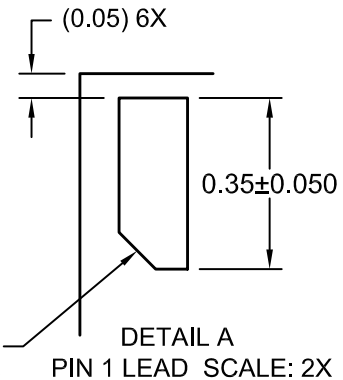
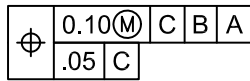


UDFN6 1.0X1.0, 0.35P
CASE 517DP
ISSUE O

DATE 31 AUG 2016



ALTERNATIVE LAND PATTERN FOR UNIVERSAL APPLICATION



NOTES:

- A. COMPLIES TO JEDEC MO-252 STANDARD
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009

0.075X45° CHAMFER
PIN 1 LEAD SCALE: 2X

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