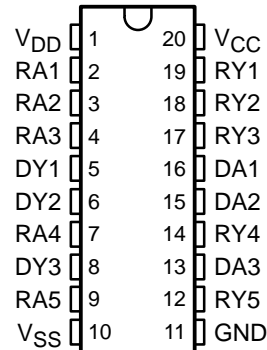


# GD65232, GD75232 MULTIPLE RS-232 DRIVERS AND RECEIVERS

SLLS206H – MAY 1995 – REVISED JUNE 2002

- **Single Chip With Easy Interface Between UART and Serial-Port Connector of IBM™ PC/AT and Compatibles**
- **Meet or Exceed the Requirements of ANSI Standard TIA/EIA-232-F and ITU Recommendation V.28**
- **Designed to Support Data Rates up to 120 kbit/s**
- **Pinout Compatible With SN75C185 and SN75185**

GD65232, GD75232 . . . DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



## description

The GD65232 and GD75232 combine three drivers and five receivers from the Texas Instruments trade-standard SN75188 and SN75189 bipolar quadruple drivers and receivers, respectively. The pinout matches the flow-through design of the SN75C185 to decrease the part count, reduce the board space required, and allow easy interconnection of the UART and serial-port connector of an IBM™ PC/AT and compatibles. The bipolar circuits and processing of the GD65232 and GD75232 provide a rugged, low-cost solution for this function at the expense of quiescent power and external passive components relative to the SN75C185.

The GD65232 and GD75232 comply with the requirements of the TIA/EIA-232-F and ITU (formerly CCITT) V.28 standards. These standards are for data interchange between a host computer and a peripheral at signaling rates up to 20 kbit/s. The switching speeds of these devices are fast enough to support rates up to 120 kbit/s with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be expected unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates up to 120 kbit/s, use of ANSI TIA/EIA-423-B (ITU V.10) and TIA/EIA-422-B (ITU V.11) standards is recommended.

## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	GD65232N	GD65232N
	SOIC – DW	Tube	GD65232DW	GD65232
		Tape and reel	GD65232DWR	
	SSOP – DB	Tape and reel	GD65232DBR	GD65232
TSSOP – PW	Tape and reel	GD65232PWR	GD65232	
0°C to 70°C	PDIP – N	Tube	GD75232N	GD75232N
	SOIC – DW	Tube	GD75232DW	GD75232
		Tape and reel	GD75232DWR	
	SSOP – DB	Tape and reel	GD75232DBR	GD75232
TSSOP – PW	Tape and reel	GD75232PWR	GD75232	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
INSTRUMENTS**

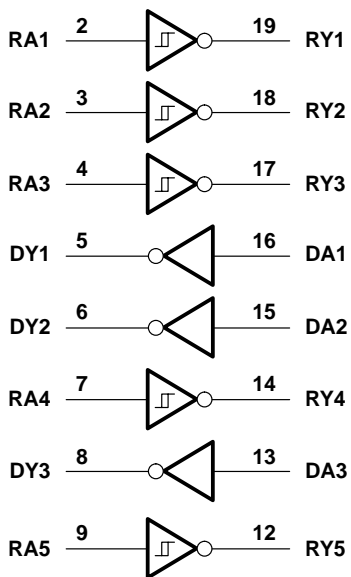
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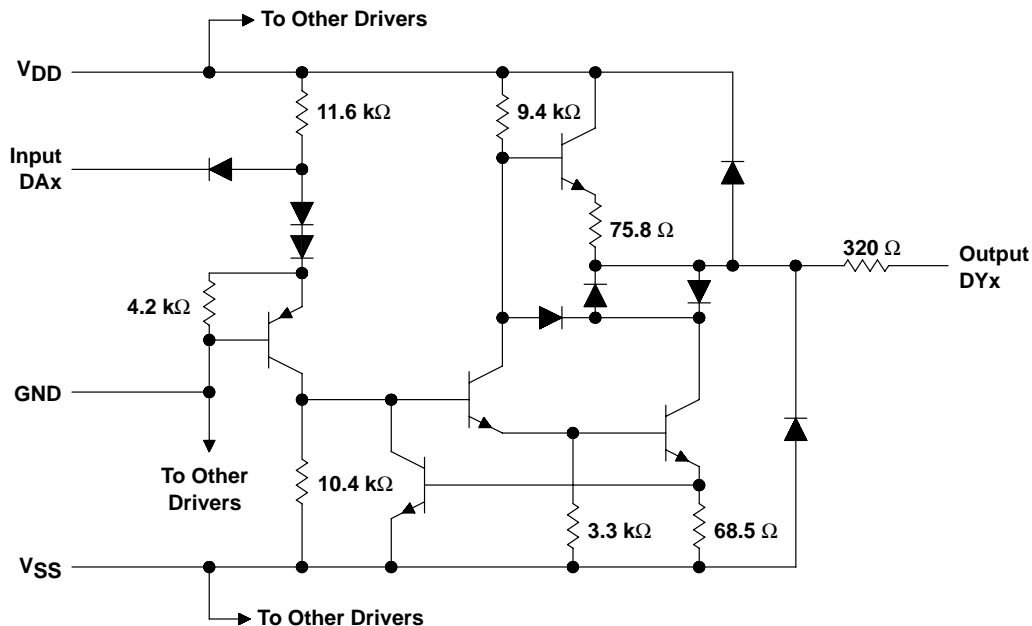
# GD65232, GD75232 MULTIPLE RS-232 DRIVERS AND RECEIVERS

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## logic diagram (positive logic)

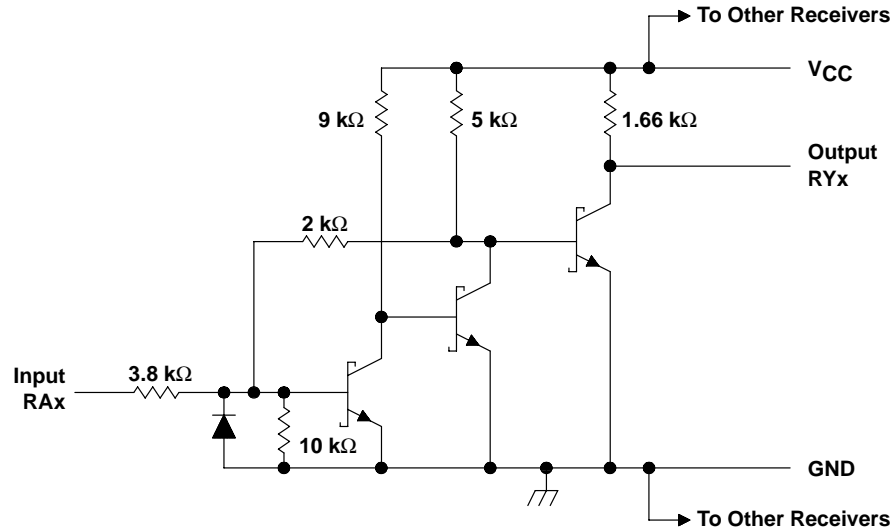


## schematic (each driver)



Resistor values shown are nominal.

**schematic (each receiver)**



Resistor values shown are nominal.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage (see Note 1): $V_{CC}$ .....	10 V
$V_{DD}$ .....	15 V
$V_{SS}$ .....	-15 V
Input voltage range, $V_I$ : Driver .....	-15 V to 7 V
Receiver .....	-30 V to 30 V
Driver output voltage range, $V_O$ .....	-15 V to 15 V
Receiver low-level output current, $I_{OL}$ .....	20 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package .....	70°C/W
DW package .....	58°C/W
N package .....	69°C/W
PW package .....	83°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .....	260°C
Storage temperature range, $T_{Stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to the network ground terminal.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

# GD65232, GD75232 MULTIPLE RS-232 DRIVERS AND RECEIVERS

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## recommended operating conditions

		MIN	NOM	MAX	UNIT
V <sub>DD</sub>	Supply voltage (see Note 3)	7.5	9	15	V
V <sub>SS</sub>	Supply voltage (see Note 3)	-7.5	-9	-15	V
V <sub>CC</sub>	Supply voltage (see Note 3)	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage (driver only)	1.9			V
V <sub>IL</sub>	Low-level input voltage (driver only)			0.8	V
I <sub>OH</sub>	High-level output current	Driver		-6	mA
		Receiver		-0.5	
I <sub>OL</sub>	Low-level output current	Driver		6	mA
		Receiver		16	
T <sub>A</sub>	Operating free-air temperature	GD65232	-40	85	°C
		GD75232	0	70	

NOTE 3: When powering up the GD65232 and GD75232, the following sequence should be used:

1. V<sub>SS</sub>
2. GND
3. V<sub>DD</sub>
4. V<sub>CC</sub>
5. I/Os

Applying V<sub>CC</sub> to the device before V<sub>DD</sub> may allow large currents to flow, causing damage to the device. When powering down the GD65232 and GD75232, the reverse sequence should be used.

## supply currents over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
I <sub>DD</sub> Supply current from V <sub>DD</sub>	All inputs at 1.9 V, No load	V <sub>DD</sub> = 9 V, V <sub>SS</sub> = -9 V		15	mA
		V <sub>DD</sub> = 12 V, V <sub>SS</sub> = -12 V		19	
		V <sub>DD</sub> = 15 V, V <sub>SS</sub> = -15 V		25	
	All inputs at 0.8 V, No load	V <sub>DD</sub> = 9 V, V <sub>SS</sub> = -9 V		4.5	
		V <sub>DD</sub> = 12 V, V <sub>SS</sub> = -12 V		5.5	
		V <sub>DD</sub> = 15 V, V <sub>SS</sub> = -15 V		9	
I <sub>SS</sub> Supply current from V <sub>SS</sub>	All inputs at 1.9 V, No load	V <sub>DD</sub> = 9 V, V <sub>SS</sub> = -9 V		-15	mA
		V <sub>DD</sub> = 12 V, V <sub>SS</sub> = -12 V		-19	
		V <sub>DD</sub> = 15 V, V <sub>SS</sub> = -15 V		-25	
	All inputs at 0.8 V, No load	V <sub>DD</sub> = 9 V, V <sub>SS</sub> = -9 V		-3.2	
		V <sub>DD</sub> = 12 V, V <sub>SS</sub> = -12 V		-3.2	
		V <sub>DD</sub> = 15 V, V <sub>SS</sub> = -15 V		-3.2	
I <sub>CC</sub> Supply current from V <sub>CC</sub>	All inputs at 5 V, No load, V <sub>CC</sub> = 5 V	GD65232		38	mA
		GD75232		30	



**DRIVER SECTION**

**electrical characteristics over recommended operating free-air temperature range,  $V_{DD} = 9\text{ V}$ ,  $V_{SS} = -9\text{ V}$ ,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$V_{IL} = 0.8\text{ V}$ ,	$R_L = 3\text{ k}\Omega$ ,	See Figure 1	6	7.5		V
$V_{OL}$	Low-level output voltage (see Note 4)	$V_{IH} = 1.9\text{ V}$ ,	$R_L = 3\text{ k}\Omega$ ,	See Figure 1		-7.5	-6	V
$I_{IH}$	High-level input current	$V_I = 5\text{ V}$ ,		See Figure 2			10	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_I = 0$ ,		See Figure 2			-1.6	$\text{mA}$
$I_{OS(H)}$	High-level short-circuit output current (see Note 5)	$V_{IL} = 0.8\text{ V}$ ,	$V_O = 0$ ,	See Figure 1	-4.5	-12	-19.5	$\text{mA}$
$I_{OS(L)}$	Low-level short-circuit output current	$V_{IH} = 2\text{ V}$ ,	$V_O = 0$ ,	See Figure 1	4.5	12	19.5	$\text{mA}$
$r_o$	Output resistance (see Note 6)	$V_{CC} = V_{DD} = V_{SS} = 0$ ,		$V_O = -2\text{ V to } 2\text{ V}$	300			$\Omega$

- NOTES: 4. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only (e.g., if  $-10\text{ V}$  is maximum, the typical value is a more negative voltage).  
5. Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.  
6. Test conditions are those specified by TIA/EIA-232-F and as listed above.

**switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $V_{DD} = 12\text{ V}$ ,  $V_{SS} = -12\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low- to high-level output	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ ,	$C_L = 15\text{ pF}$ ,	See Figure 3		315	500	ns
$t_{PHL}$	Propagation delay time, high- to low-level output	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ ,	$C_L = 15\text{ pF}$ ,	See Figure 3		75	175	ns
$t_{TLH}$	Transition time, low- to high-level output	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$	$C_L = 15\text{ pF}$ ,	See Figure 3		60	100	ns
			$C_L = 2500\text{ pF}$ ,	See Figure 3 and Note 7		1.7	2.5	$\mu\text{s}$
$t_{THL}$	Transition time, high- to low-level output	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$	$C_L = 15\text{ pF}$ ,	See Figure 3		40	75	ns
			$C_L = 2500\text{ pF}$ ,	See Figure 3 and Note 7		1.5	2.5	$\mu\text{s}$

NOTE 7: Measured between  $\pm 3\text{-V}$  and  $\pm 3\text{-V}$  points of the output waveform (TIA/EIA-232-F conditions); all unused inputs are tied either high or low.

# GD65232, GD75232 MULTIPLE RS-232 DRIVERS AND RECEIVERS

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## RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IT+</sub>	Positive-going input threshold voltage	T <sub>A</sub> = 25°C,	See Figure 5	1.75	1.9	2.3	V
		T <sub>A</sub> = 0°C to 70°C,	See Figure 5	1.55		2.3	
V <sub>IT-</sub>	Negative-going input threshold voltage			0.75	0.97	1.25	V
V <sub>hys</sub>	Input hysteresis voltage (V <sub>IT+</sub> – V <sub>IT-</sub> )			0.5			V
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = –0.5 mA	V <sub>IH</sub> = 0.75 V	2.6	4	5	V
			Inputs open	2.6			
V <sub>OL</sub>	Low-level input voltage	I <sub>OL</sub> = 10 mA,	V <sub>I</sub> = 3 V		0.2	0.45	V
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = 25 V,	See Figure 5	GD65232	3.6	11	mA
				GD75232	3.6	8.3	
		V <sub>I</sub> = 3 V,	See Figure 5	0.43			
I <sub>IL</sub>	Low-level output current	V <sub>I</sub> = –25 V,	See Figure 5	GD65232	–3.6	–11	mA
				GD75232	–3.6	–8.3	
		V <sub>I</sub> = –3 V,	See Figure 5	–0.43			
I <sub>OS</sub>	Short-circuit output current	See Figure 4			–3.4	–12	mA

† All typical values are at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5 V, V<sub>DD</sub> = 9 V, and V<sub>SS</sub> = –9 V.

switching characteristics, V<sub>CC</sub> = 5 V, V<sub>DD</sub> = 12 V, V<sub>SS</sub> = –12 V, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 5 kΩ, See Figure 6			107	250	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output				42	150	ns
t <sub>TLH</sub>	Transition time, low- to high-level output				175	350	ns
t <sub>THL</sub>	Transition time, high- to low-level output				16	60	ns
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1.5 kΩ, See Figure 6			100	160	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output				60	100	ns
t <sub>TLH</sub>	Transition time, low- to high-level output				90	175	ns
t <sub>THL</sub>	Transition time, high- to low-level output				15	50	ns



PARAMETER MEASUREMENT INFORMATION

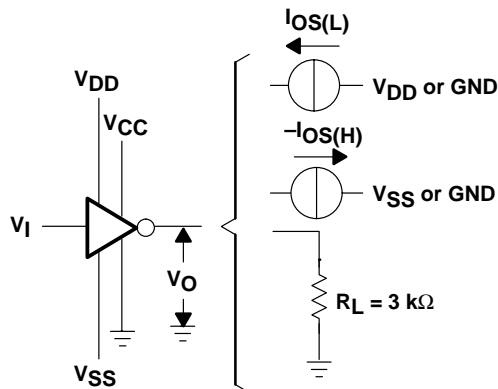


Figure 1. Driver Test Circuit for  $V_{OH}$ ,  $V_{OL}$ ,  $I_{OS(H)}$ , and  $I_{OS(L)}$

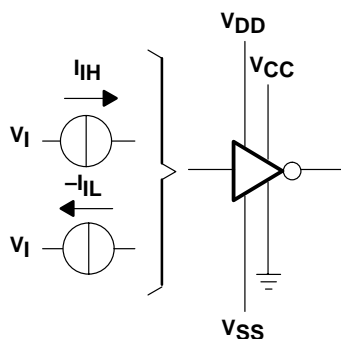
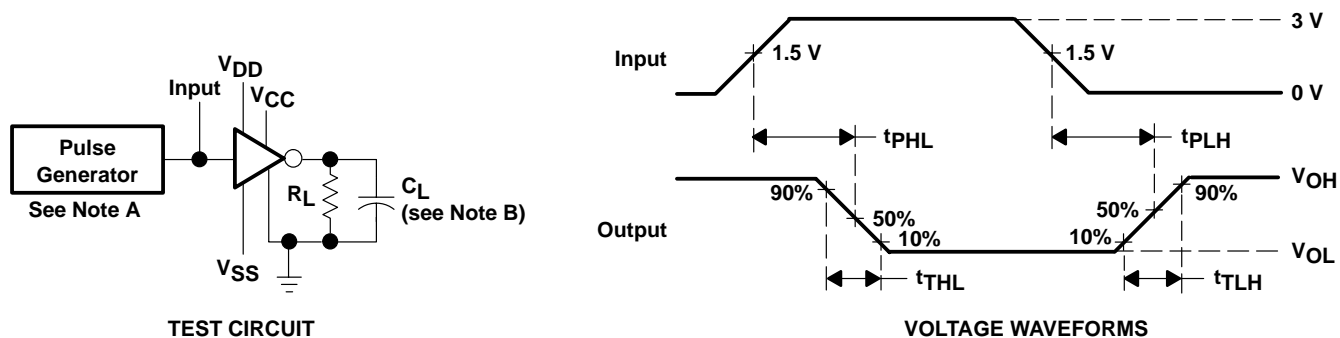


Figure 2. Driver Test Circuit for  $I_{IH}$  and  $I_{IL}$



NOTES: A. The pulse generator has the following characteristics:  $t_w = 25\ \mu\text{s}$ ,  $\text{PRR} = 20\ \text{kHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = t_f < 50\ \text{ns}$ .  
 B.  $C_L$  includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

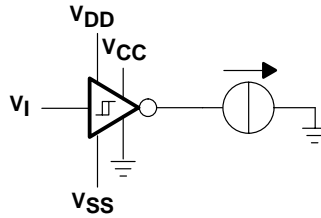


Figure 4. Receiver Test Circuit for  $I_{0S}$

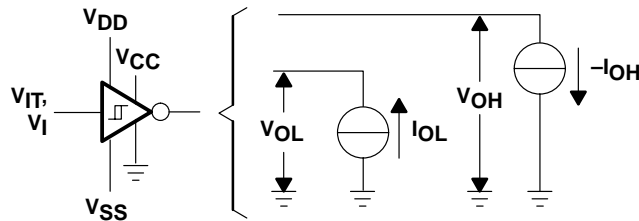
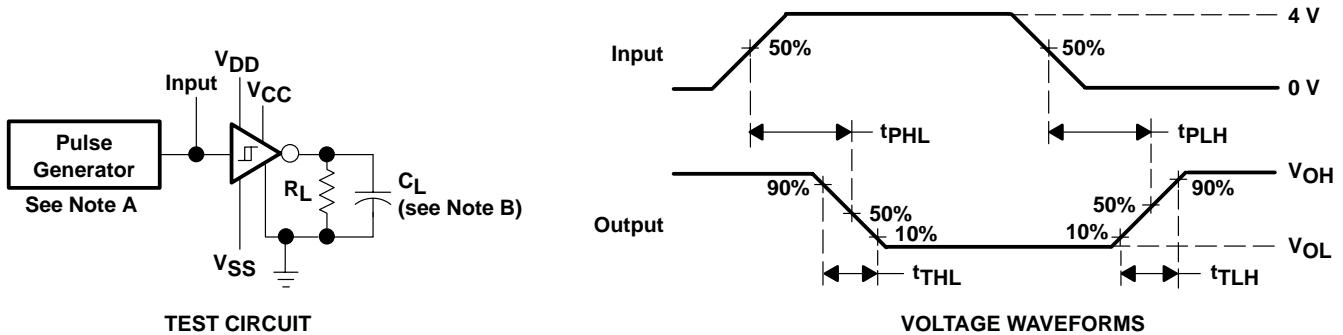


Figure 5. Receiver Test Circuit for  $V_{IT}$ ,  $V_{OH}$ , and  $V_{OL}$



NOTES: A. The pulse generator has the following characteristics:  $t_w = 25 \mu s$ , PRR = 20 kHz,  $Z_O = 50 \Omega$ ,  $t_r = t_f < 50 ns$ .  
 B.  $C_L$  includes probe and jig capacitance.

Figure 6. Receiver Propagation and Transition Times



TYPICAL CHARACTERISTICS

DRIVER SECTION

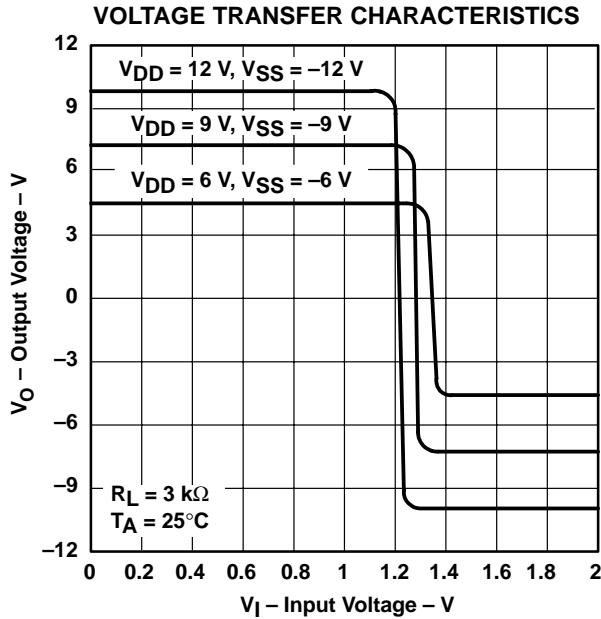


Figure 7

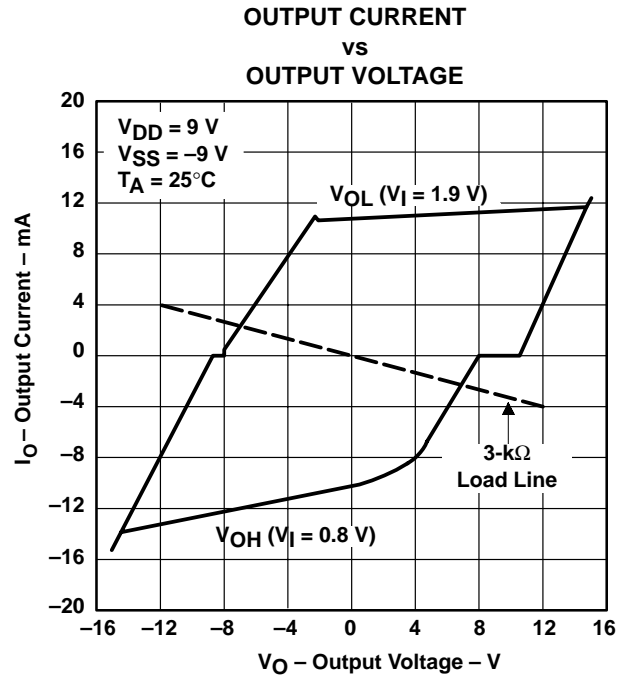


Figure 8

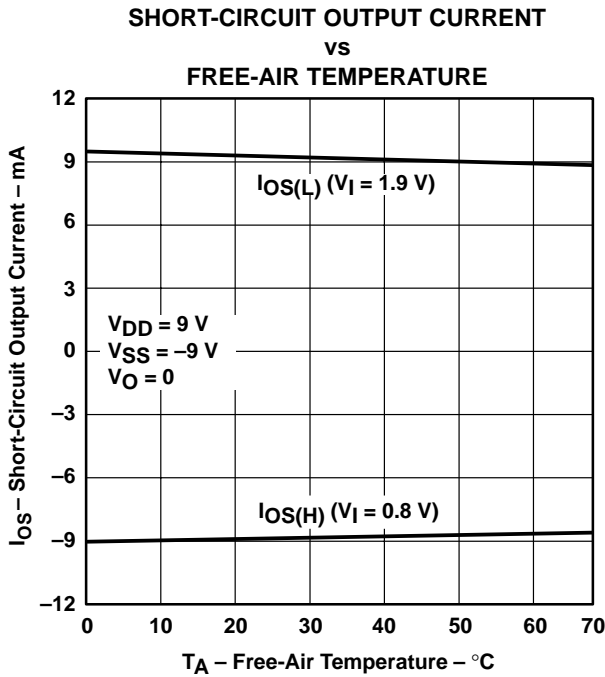


Figure 9

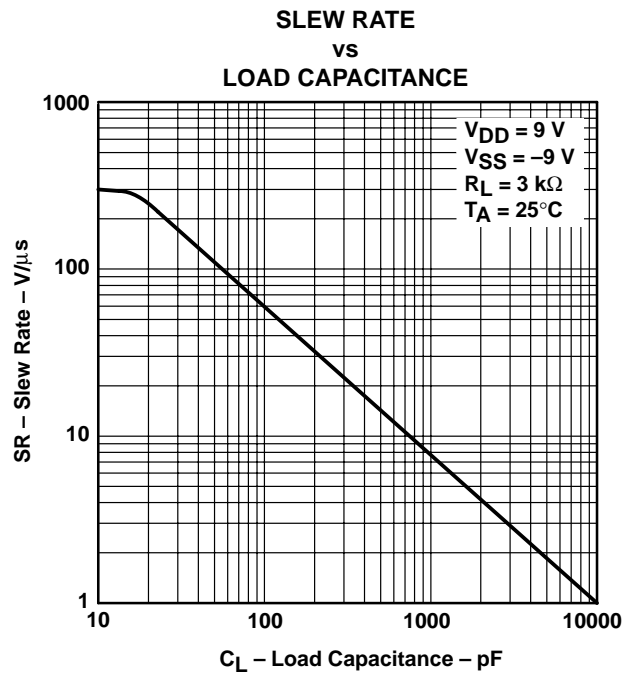


Figure 10

TYPICAL CHARACTERISTICS

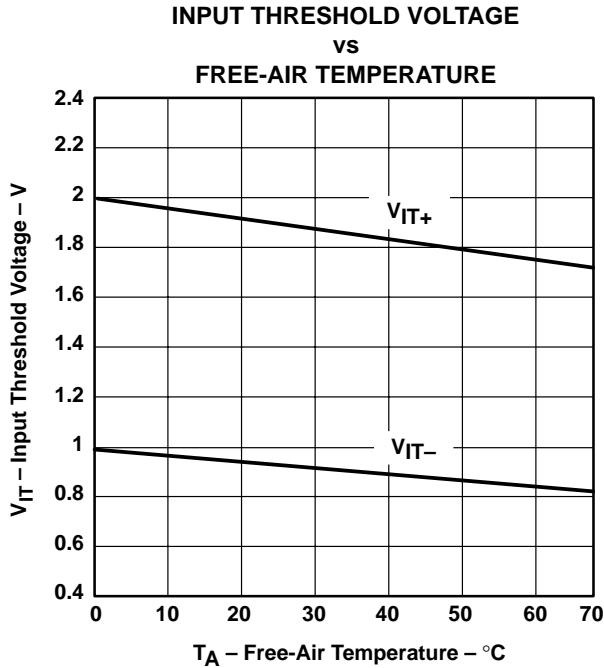


Figure 11

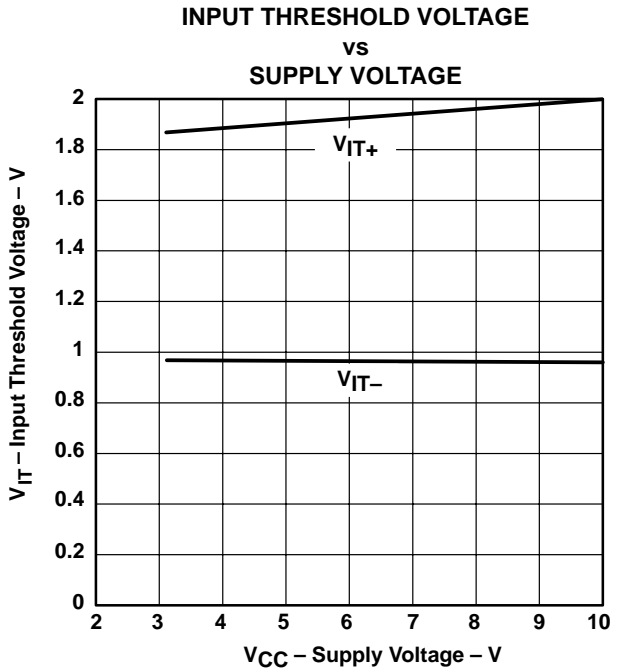
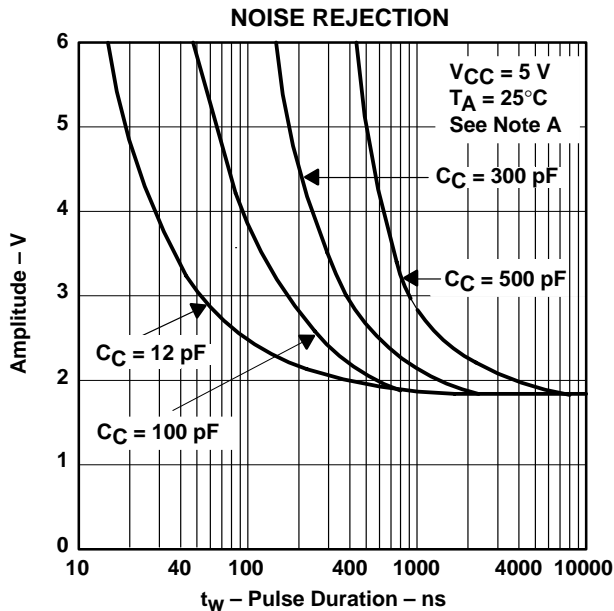


Figure 12



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, does not cause a change of the output level.

Figure 13

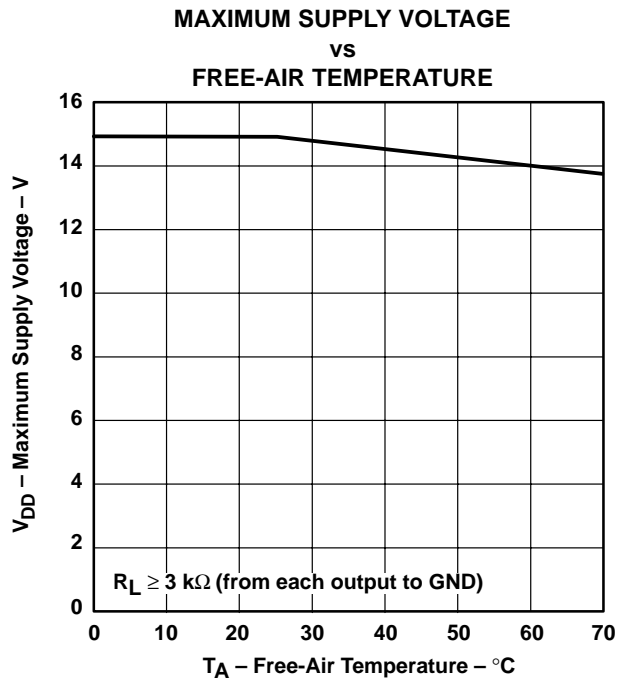
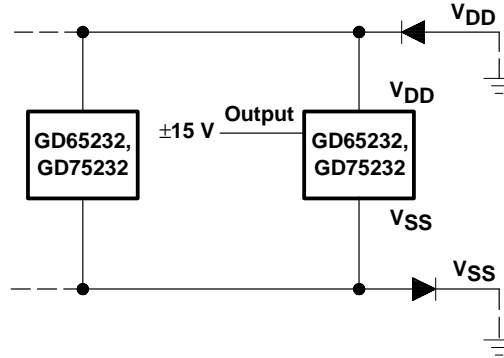


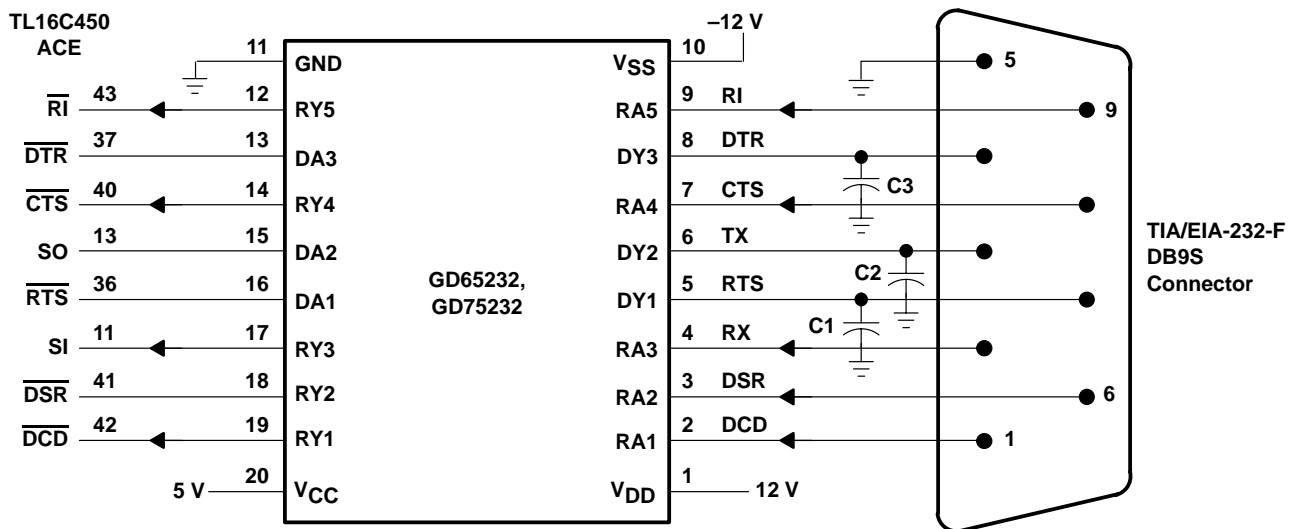
Figure 14

**APPLICATION INFORMATION**

Diodes placed in series with the  $V_{DD}$  and  $V_{SS}$  leads protect the GD65232 and GD75232 in the fault condition in which the device outputs are shorted to  $\pm 15$  V and the power supplies are at low and provide low-impedance paths to ground (see Figure 15).



**Figure 15. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F**



**Figure 16. Typical Connection**

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