BURR-BROWN®

DDC112

Dual Current Input 20-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- MONOLITHIC CHARGE MEASUREMENT ADC
- DIGITAL FILTER NOISE REDUCTION: 3.2ppm, rms
- INTEGRAL LINEARITY: ±0.005% Reading ±0.5ppm FSR
- HIGH PRECISION, TRUE INTEGRATING FUNCTION
- PROGRAMMABLE FULL SCALE
- SINGLE SUPPLY
- CASCADABLE OUTPUT

APPLICATIONS

- DIRECT PHOTOSENSOR DIGITIZATION
- CT SCANNER DAS
- INFRARED PYROMETER
- PRECISION PROCESS CONTROL
- LIQUID/GAS CHROMATOGRAPHY
- BLOOD ANALYSIS

DESCRIPTION

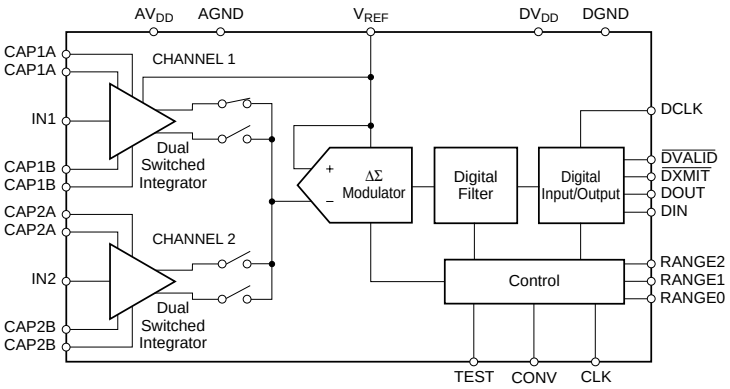
The DDC112 is a dual input, wide dynamic range, charge digitizing analog-to-digital converter (ADC) with 20-bit resolution. Low level current output devices, such as photosensors, can be directly connected to its inputs. Charge integration is continuous as each input uses two integrators; while one is being digitized, the other is integrating.

For each of its two inputs, the DDC112 combines current-to-voltage conversion, continuous integration, programmable full-scale range, A/D conversion, and digital filtering to achieve a precision, wide dynamic range digital result. In addition to the internal programmable full-scale ranges, external integrating capacitors allow an additional user-settable full-scale range of up to 1000pC.

To provide single-supply operation, the internal ADC utilizes a differential input, with the positive input tied to V_{REF}. When the integration capacitor is reset at the beginning of each integration cycle, the capacitor charges to V_{REF}. This charge is removed in proportion to the input current. At the end of the integration cycle, the remaining voltage is compared to V_{REF}.

The high-speed serial shift register which holds the result of the last conversion can be configured to allow multiple DDC112 units to be cascaded, minimizing interconnections. The DDC112 is available in a 28-lead SOIC package and is guaranteed over the –40°C to +85°C temperature range.

Patents Pending



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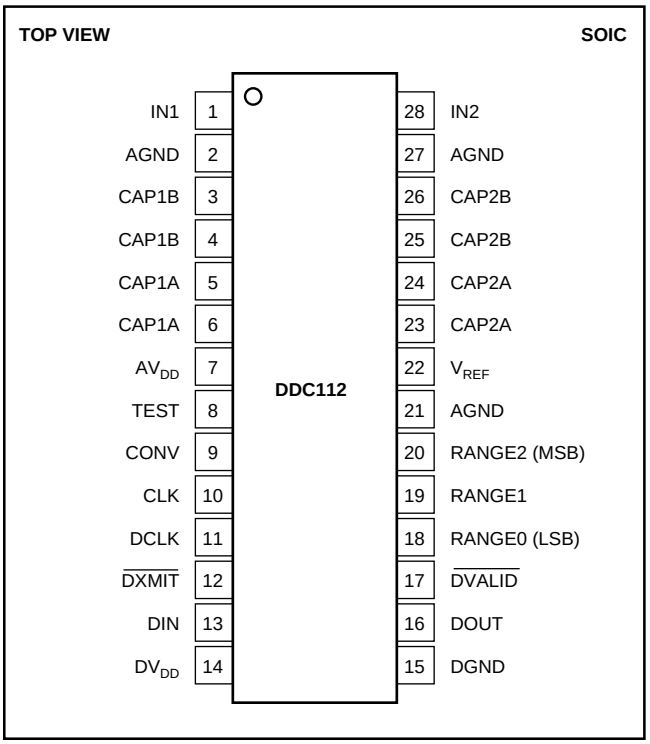
SPECIFICATIONS

At T_A = +25°C, AV_{DD} = DV_{DD} = +5V, T_{INT} = 500µs, CLK = 10MHz, V_{REF} = +4.096V, continuous mode operation, and internal integration capacitors, unless otherwise noted.

PARAMETER	CONDITIONS	DDC112 MIN	DDC112 TYP	DDC112 MAX	UNITS
ANALOG INPUTS					
External, Positive Full-Scale					
Range 0	C_{EXT} = 250pF			1000	pC
Internal, Positive Full-Scale					
Range 1		47.5	50	52.5	pC
Range 2		95	100	105	pC
Range 3		142.5	150	157.5	pC
Range 4		190	200	210	pC
Range 5		237.5	250	262.5	pC
Range 6		285	300	315	pC
Range 7		332.5	350	367.5	pC
Negative Full-Scale Input			–0.4% of Positive FS		pC
DYNAMIC CHARACTERISTICS					
Conversion Rate				2	kHz
Integration Time, T_{INT}	Continuous Mode	500		1,000,000	µs
Integration Time, T_{INT}	Non-continuous Mode	50			µs
System Clock Input (CLK)		5	10	12	MHz
Data Clock (DCLK)				12	MHz
ACCURACY					
Noise, Low Level Current Input[1]	C_{SENSOR}[2] = 0pF, Range 5 (250pC)		3.2		ppm of FSR[3], rms
	C_{SENSOR} = 25pF, Range 5 (250pC)		3.8		ppm of FSR, rms
	C_{SENSOR} = 50pF, Range 5 (250pC)		4.2	6.0	ppm of FSR, rms
Differential Linearity Error			±0.005% Reading ±0.5ppm FSR, max		
Integral Linearity Error[4]			±0.005% Reading ±0.5ppm FSR, typ		
			±0.025% Reading ±1.0ppm FSR, max		
No Missing Codes			20		Bits
Input Bias Current	T_A = +25°C		0.1	10	pA
Range Error	Range 5 (250pC)			5	% of FSR
Range Error Match[5]	All Ranges		0.1	0.5	% of FSR
Range Sensitivity to V_{REF}	V_{REF} = 4.096 ±0.1V		1:1		
Offset Error	Range 5, (250pC)		±200		ppm of FSR
Offset Error Match[5]			±100		ppm of FSR
DC Bias Voltage[6] (Input V_{OS})			±0.05	±2	mV
Power Supply Rejection Ratio			±25	±200	ppm/V
Internal Test Signal			13		pC
Internal Test Accuracy			±10		%
PERFORMANCE OVER TEMPERATURE					
Offset Drift			±0.5		ppm/°C
Offset Drift Stability			±0.02		ppm/minute
DC Bias Voltage Drift	Applied to Sensor Input		3		µV/°C
Input Bias Current Drift	+25°C to +45°C		0.01	1	pA/°C
Input Bias Current	T_A = +75°C		2	50	pA
Range Drift[7]	Range 5 (250pC)		±20		ppm/°C
Range Drift Match[5]	Range 5 (250pC)		±0.05		ppm/°C
REFERENCE					
Voltage		4.000	4.096	4.200	V
Input Current[8]	T_{INT} = 500µs		150		µA
DIGITAL INPUT/OUTPUT					
Logic Levels					
V_{IH}		4.0		DV_{DD} +0.3	V
V_{IL}		–0.3		+0.8	V
V_{OH}	I_{OH} = –500µA	4.5			V
V_{OL}	I_{OL} = 500µA			0.4	V
Input Current, I_{IN}		–10		+10	µA
Data Format[9]			Straight Binary		
POWER SUPPLY REQUIREMENTS					
Power Supply Voltage	AV_{DD} and DV_{DD}	4.75		5.25	V
Supply Current					
Analog Current	AV_{DD} = +5V		14.8		mA
Digital Current	DV_{DD} = +5V		1.2		mA
Total Power Dissipation			80	100	mW
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C
Storage		–60		+100	°C

NOTES: (1) Input is less than 1% of full scale. (2) C_{SENSOR} is the capacitance seen at the DDC112 inputs from wiring, photodiode, etc. (3) FSR is Full-Scale Range. (4) A best-fit line is used in measuring linearity. (5) Matching between side A and side B, not input 1-to-input 2. (6) Voltage produced by the DDC112 at its input which is applied to the sensor. (7) Range drift does not include external reference drift. (8) Input reference current decreases with increasing T_{INT} (see text). (9) Data format is Straight Binary with a small offset (see text).

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS[1]

AV_{DD} to DV_{DD}	–0.3V to +6V
AV_{DD} to AGND	–0.3V to +6V
DV_{DD} to DGND	–0.3V to +6V
AGND to DGND	±0.3V
V_{REF} Voltage to AGND	–0.3V to AV_{DD} +0.3V
Digital Input Voltage to DGND	–0.3V to DV_{DD} +0.3V
Digital Output Voltage to DGND	–0.3V to DV_{DD} +0.3V
Package Power Dissipation	$(T_{JMAX} - T_A)/\theta_{JA}$
Maximum Junction Temperature (T_{JMAX})	+150°C
Thermal Resistance, θ_{JA}	150°C/W
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PIN DESCRIPTIONS

PIN	LABEL	DESCRIPTION
1	IN1	Input 1: analog input for Integrators 1A and 1B. The integrator that is active is set by the CONV input.
2	AGND	Analog Ground.
3	CAP1B	External Capacitor for Integrator 1B.
4	CAP1B	External Capacitor for Integrator 1B.
5	CAP1A	External Capacitor for Integrator 1A.
6	CAP1A	External Capacitor for Integrator 1A.
7	AV_{DD}	Analog Supply, +5V nominal.
8	TEST	Test Control Input. When HIGH, a test charge is applied to the A or B integrators on the next CONV transition.
9	CONV	Controls which side of the integrator is connected to input. In continuous mode; CONV HIGH → side A is integrating, CONV LOW → side B is integrating. CONV must be synchronized with CLK (see text).
10	CLK	System Clock Input, 10MHz nominal.
11	DCLK	Serial Data Clock Input. This input operates the serial I/O shift register.
12	$\overline{DXMIT}$	Serial Data Transmit Enable Input. When LOW, this input enables the internal serial shift register.
13	DIN	Serial Digital Input. Used to cascade multiple DDC112s.
14	DV_{DD}	Digital Supply, +5V nominal.
15	DGND	Digital Ground.
16	DOUT	Serial Data Output, Hi-Z when $\overline{DXMIT}$ is HIGH.
17	$\overline{DVALID}$	Data Valid Output. A LOW value indicates valid data is available in the serial I/O register.
18	RANGE0	Range Control Input 0 (least significant bit).
19	RANGE1	Range Control Input 1.
20	RANGE2	Range Control Input 2 (most significant bit).
21	AGND	Analog Ground.
22	V_{REF}	External Reference Input, +4.096V nominal.
23	CAP2A	External Capacitor for Integrator 2A.
24	CAP2A	External Capacitor for Integrator 2A.
25	CAP2B	External Capacitor for Integrator 2B.
26	CAP2B	External Capacitor for Integrator 2B.
27	AGND	Analog Ground.
28	IN2	Input 2: analog input for Integrators 2A and 2B. The integrator that is active is set by the CONV input.

PACKAGE/ORDERING INFORMATION

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR	SPECIFICATION TEMPERATURE RANGE	PACKAGE	PACKAGE DRAWING NUMBER[1]	ORDERING NUMBER[2]	TRANSPORT MEDIA
DDC112U	±0.025% Reading ±1.0ppm FSR	–40°C to +85°C	28-Lead SOIC	217	DDC112U	Rails
"	"	"	"	"	DDC112U/1K	Tape and Reel

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "DDC112U/1K" will get a single 1000-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

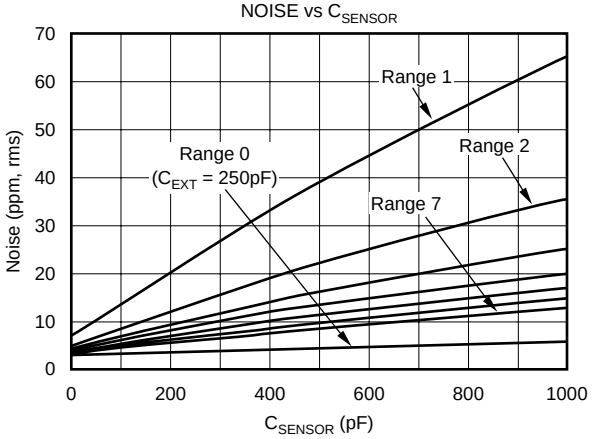
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

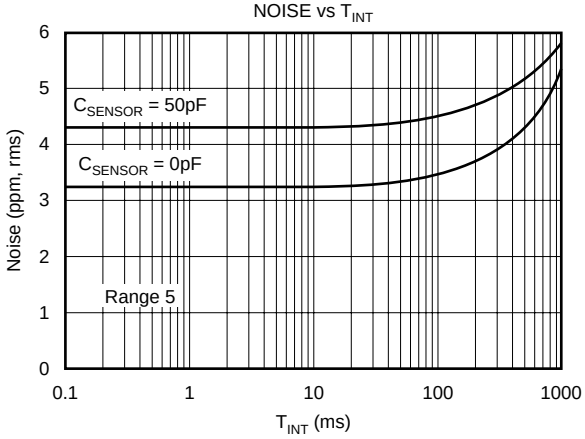
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, characterization done with Range 5 (250pC), T_{INT} = 500µs, V_{REF} = +4.096, AV_{DD} = DV_{DD} = +5V, and CLK = 10MHz, unless otherwise noted.

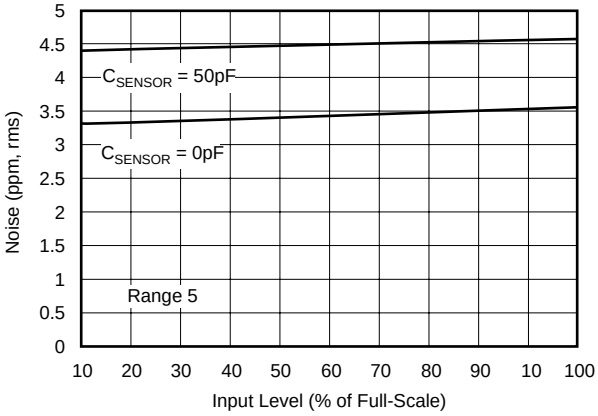
NOISE vs C_{SENSOR}



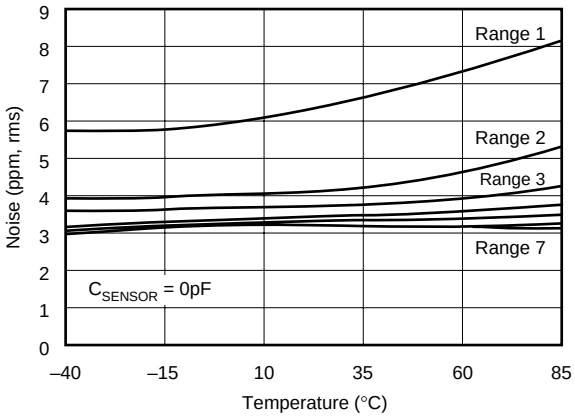
NOISE vs T_{INT}



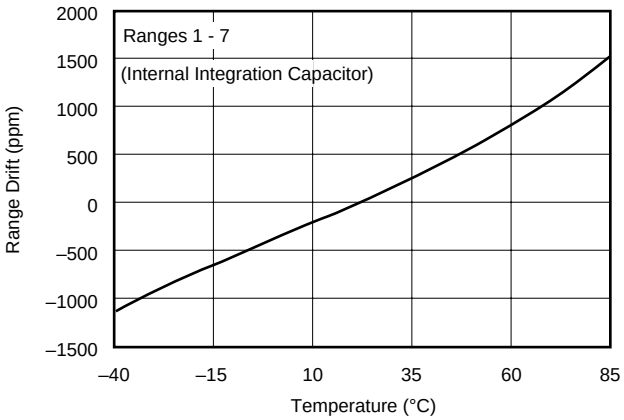
NOISE vs INPUT LEVEL



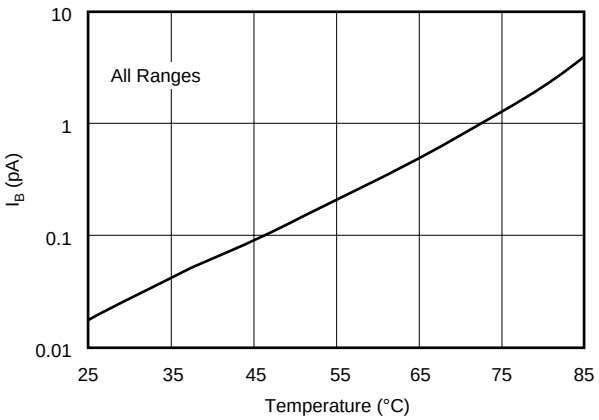
NOISE vs TEMPERATURE



RANGE DRIFT vs TEMPERATURE



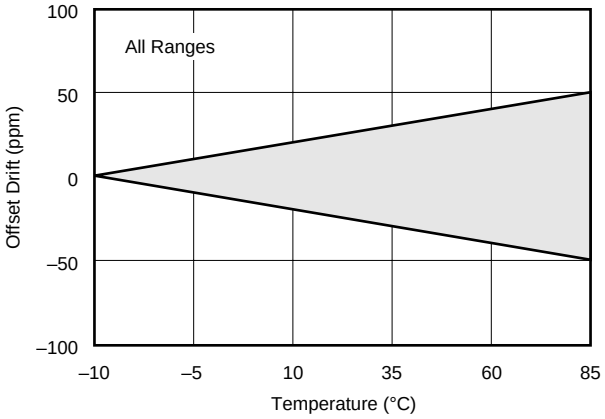
I_B vs TEMPERATURE



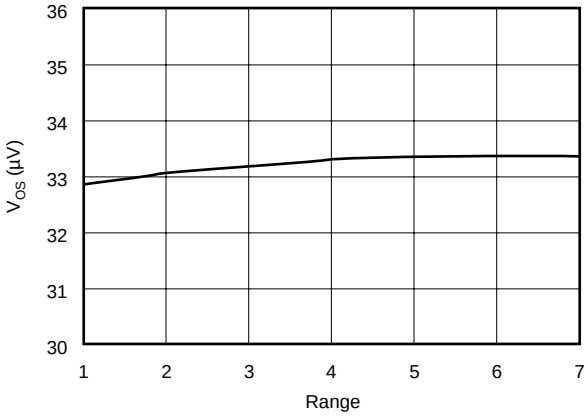
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, characterization done with Range 5 (250pC), T_{INT} = 500µs, V_{REF} = +4.096, AV_{DD} = DV_{DD} = +5V, and CLK = 10MHz, unless otherwise noted.

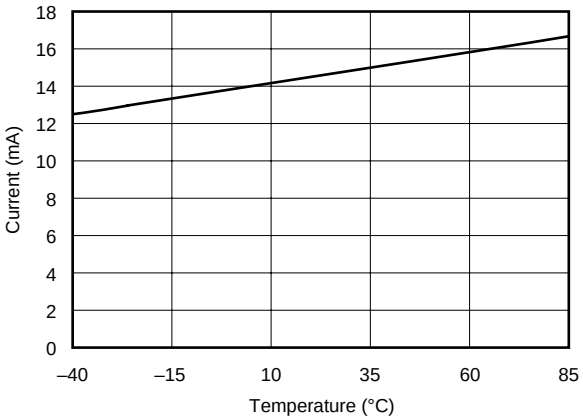
OFFSET DRIFT vs TEMPERATURE



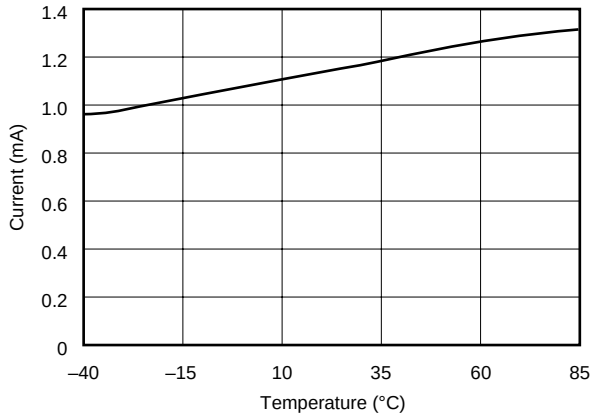
INPUT V_{OS} vs RANGE



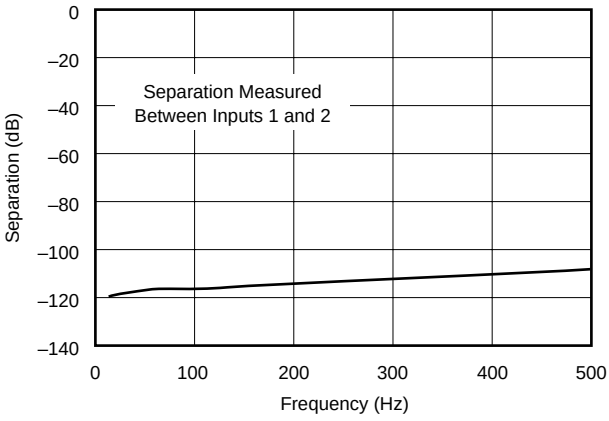
ANALOG SUPPLY CURRENT vs TEMPERATURE



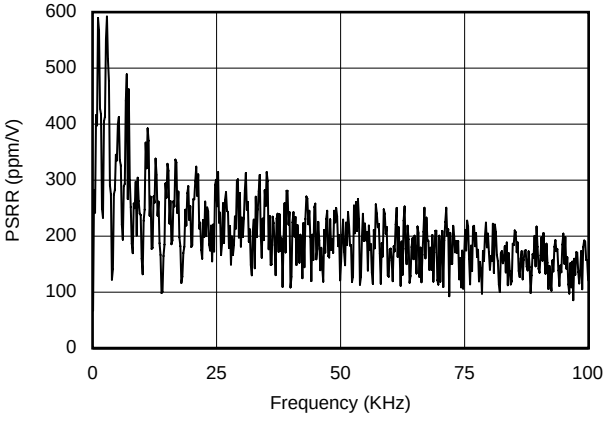
DIGITAL SUPPLY CURRENT vs TEMPERATURE



CROSSTALK vs FREQUENCY



POWER SUPPLY REJECTION RATIO vs FREQUENCY



THEORY OF OPERATION

The basic operation of the DDC112 is illustrated in Figure 1. The device contains two identical input channels where each performs the function of current-to-voltage integration followed by a multiplexed analog-to-digital (A/D) conversion. Each input has two integrators so that the current-to-voltage integration can be continuous in time. The output of the four integrators are switched to one delta-sigma converter via a four input multiplexer. With the DDC112 in the continuous integration mode, the output of the integrators from one side of both of the inputs will be digitized while the other two integrators are in the integration mode as illustrated in the timing diagram in Figure 2. This integration and A/D conversion process is controlled by the system clock, CLK. With a 10MHz system clock, the integrator combined with the delta-sigma converter accomplishes a single 20-bit conversion in approximately 220µs. The results from side A and side B of each signal input are stored in a serial output shift register. The $\overline{\text{DVALID}}$ output goes LOW when the shift register contains valid data.

The digital interface of the DDC112 provides the digital results via an asynchronous serial interface consisting of a data clock (DCLK), a transmit enable pin ($\overline{\text{DXMIT}}$), a valid data pin ($\overline{\text{DVALID}}$), a serial data output pin (DOUT), and a serial data input pin (DIN). The DDC112 contains only one A/D converter, so the conversion process is interleaved between the two inputs as shown in Figure 2. The integration and conversion process is fundamentally independent of the data retrieval process. Consequently, the CLK frequency and DCLK frequencies need not be the same. DIN is only used when multiple converters are cascaded and should be tied to DGND otherwise. Depending on T_{INT}, CLK, and DCLK, it is possible to daisy chain over 100 converters. This greatly simplifies the interconnection and routing of the digital outputs in those cases where a large number of converters are needed.

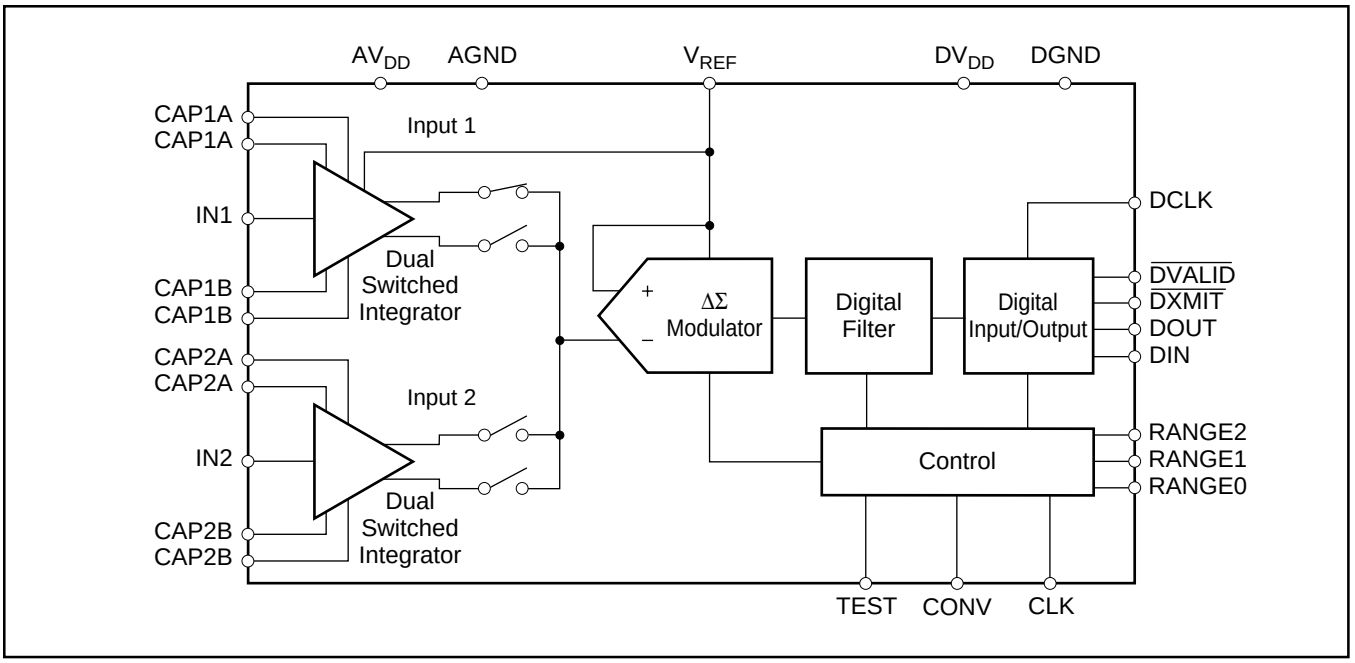


FIGURE 1. DDC112 Block Diagram.

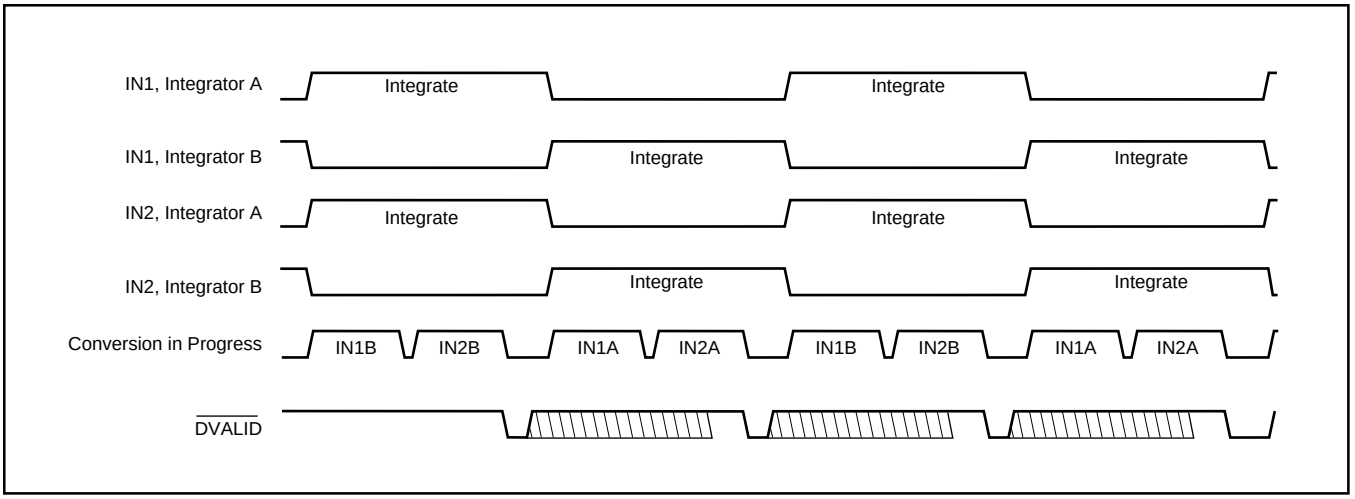


FIGURE 2. Basic Integration and Conversion Timing for the DDC112 (continuous mode).

DEVICE OPERATION

Basic Integration Cycle

The fundamental topology of the front end of the DDC112 is a classical analog integrator as shown in Figure 3. In this diagram only Input 1 is shown. This representation of the input stage consists of an operational amplifier, a selectable feedback capacitor network (C_F), and several switches that implement the integration cycle. The timing relationships of all of the switches shown in Figure 3 are illustrated in Figure 4. Figure 4 is used to conceptualize the operation of the integrator input stage of the DDC112 and should not be used as an exact timing tool for design. Block diagrams of the reset, integrate, converter and wait states of the integrator section of the DDC112 are shown in Figure 5. This internal switching network is controlled externally with the convert command (CONV), range selection pins (RANGE0-RANGE2), and the system clock (CLK). For the best noise performance, CONV must be synchronized with the rising edge of CLK. That is, CONV must toggle on the rising edge of CLK.

The non-inverting inputs of the integrators are internally referenced to ground. Consequently, the DDC112 analog ground should be as clean as possible. The range switches, along with the internal and external capacitors (C_F) are shown in parallel between the inverting input and output of the operational amplifier. Table I shows the value of the integration capacitor (C_F) for each range. At the beginning of a conversion, the switches $S_{A/D}$, S_{INTA}, S_{INTB}, S_{REF1}, S_{REF2}, and S_{RESET} are set as shown in Figure 4.

At the completion of an A/D conversion, the charge on the integration capacitor (C_F) is reset with S_{REF1} and S_{RESET} (Figures 4 and 5a). This is done during the reset time. In this manner, the selected capacitor is charged to the reference voltage, V_{REF}. Once the integration capacitor is charged, S_{REF1}, and S_{RESET} are switched so that V_{REF} is no longer connected to the amplifier circuit while it waits to begin integrating (Figure 5b). With the rising edge on CONV, S_{INTA} closes which begins the integration of Channel A. This puts the integrator stage into its integrate mode (Figure 5c).

Charge from the input signal is collected on the integration capacitor causing the voltage output of the amplifier to decrease. A falling edge CONV stops the integration by switching the input signal from side A to side B (S_{INTA} and S_{INTB}). Prior to the falling edge of CONV, the signal on side B was converted by the A/D converter and reset during the time that side A was integrating. With the falling edge of CONV, side B starts integrating the input signal. Now the output voltage of side A's operational amplifier is presented to the input of the ΔΣ A/D converter (as shown in Figure 5d).

RANGE2	RANGE1	RANGE0	C_F (pF, typ)	INPUT RANGE (pC, typ)
0	0	0	External 12.5 to 250	Up to 1000
0	0	1	12.5	–0.2 to 50
0	1	0	25	–0.4 to 100
0	1	1	37.5	–0.6 to 150
1	0	0	50	–0.8 to 200
1	0	1	62.5	–0.1 to 250
1	1	0	75	–1.2 to 300
1	1	1	87.5	–1.4 to 350

TABLE I. Range Selection of the DDC112.

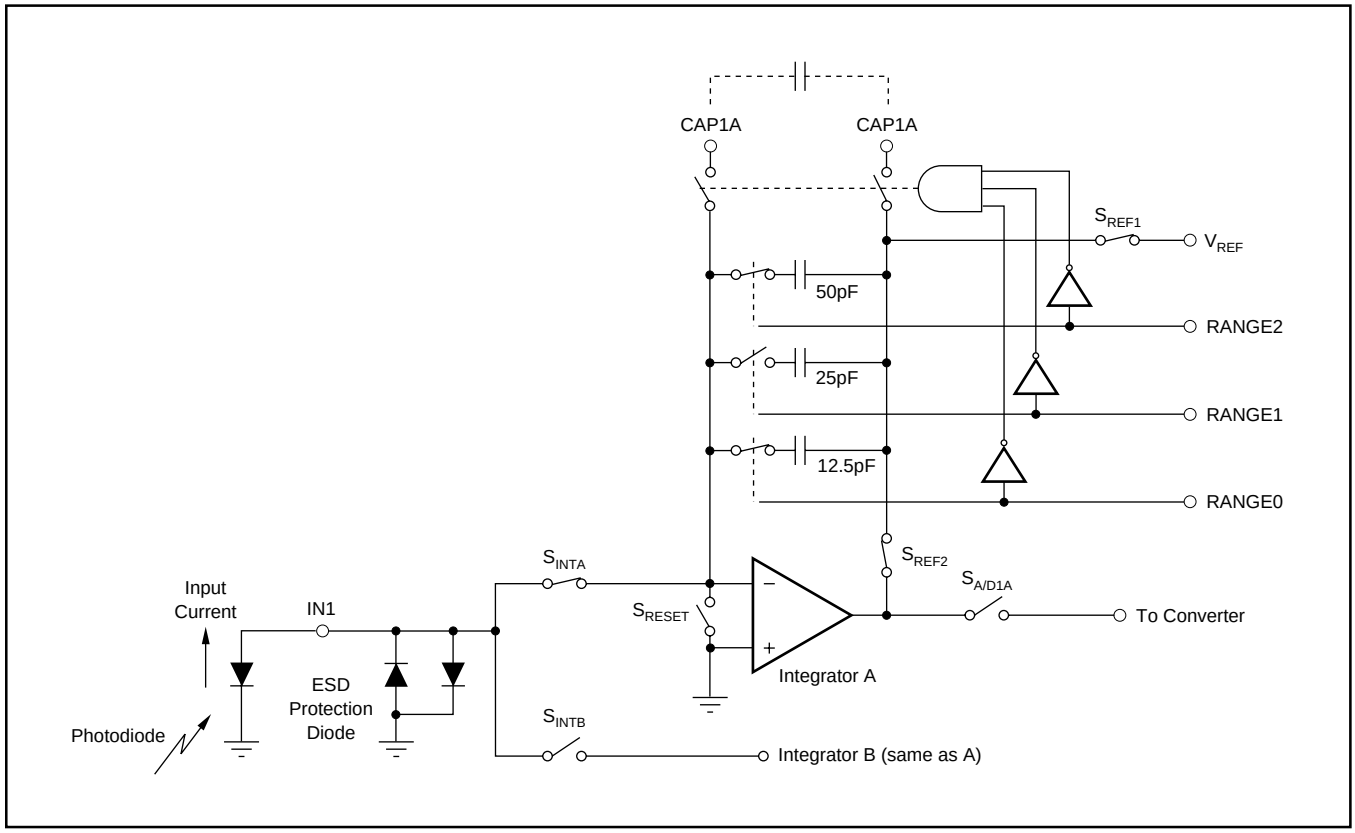


FIGURE 3. Basic Integrator Configuration for Input 1 Shown with a 250pC (C_F = 62.5pF) Input Range.

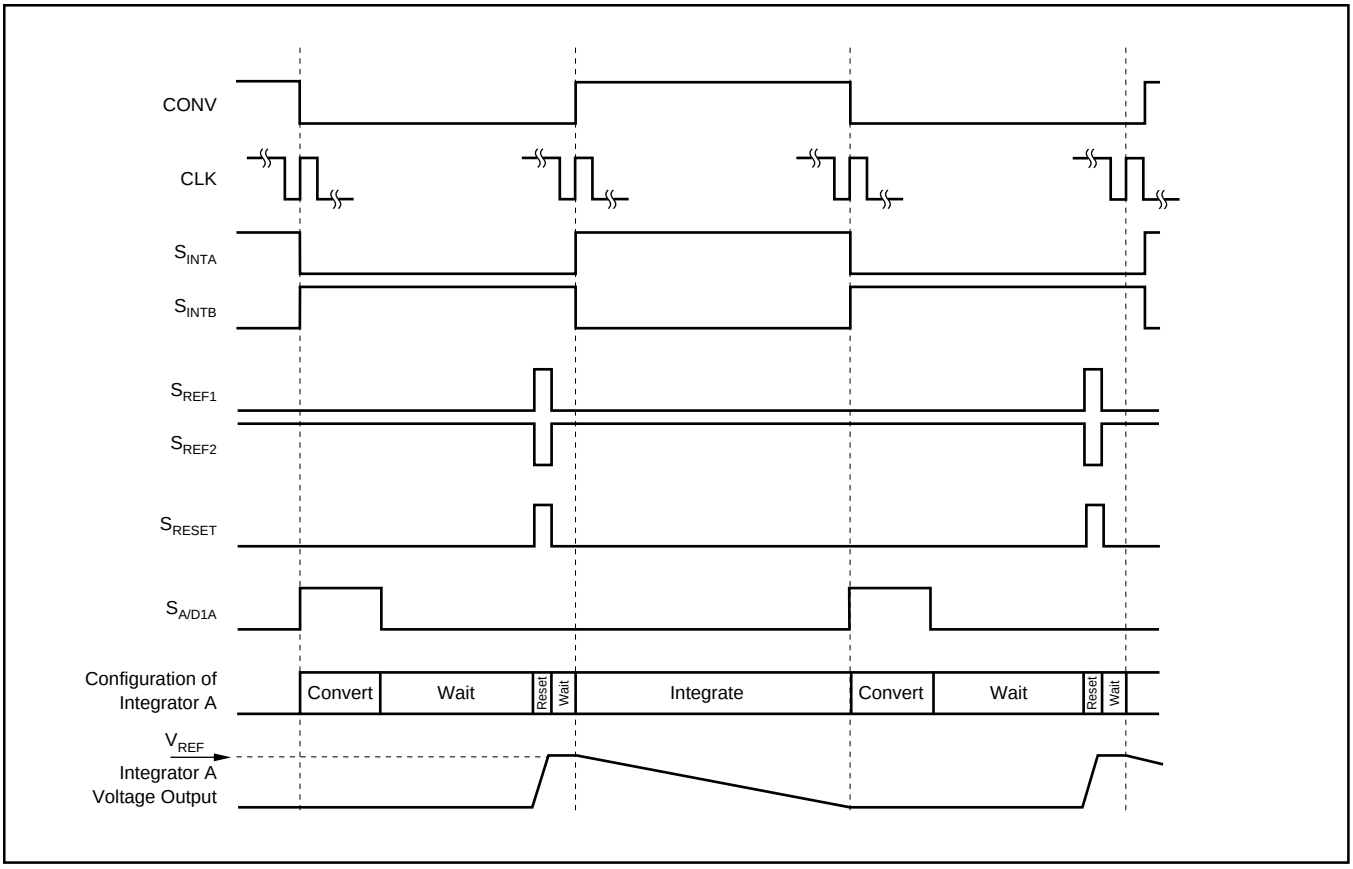


FIGURE 4. Basic Integrator Timing Diagram as Illustrated in Figure 3.

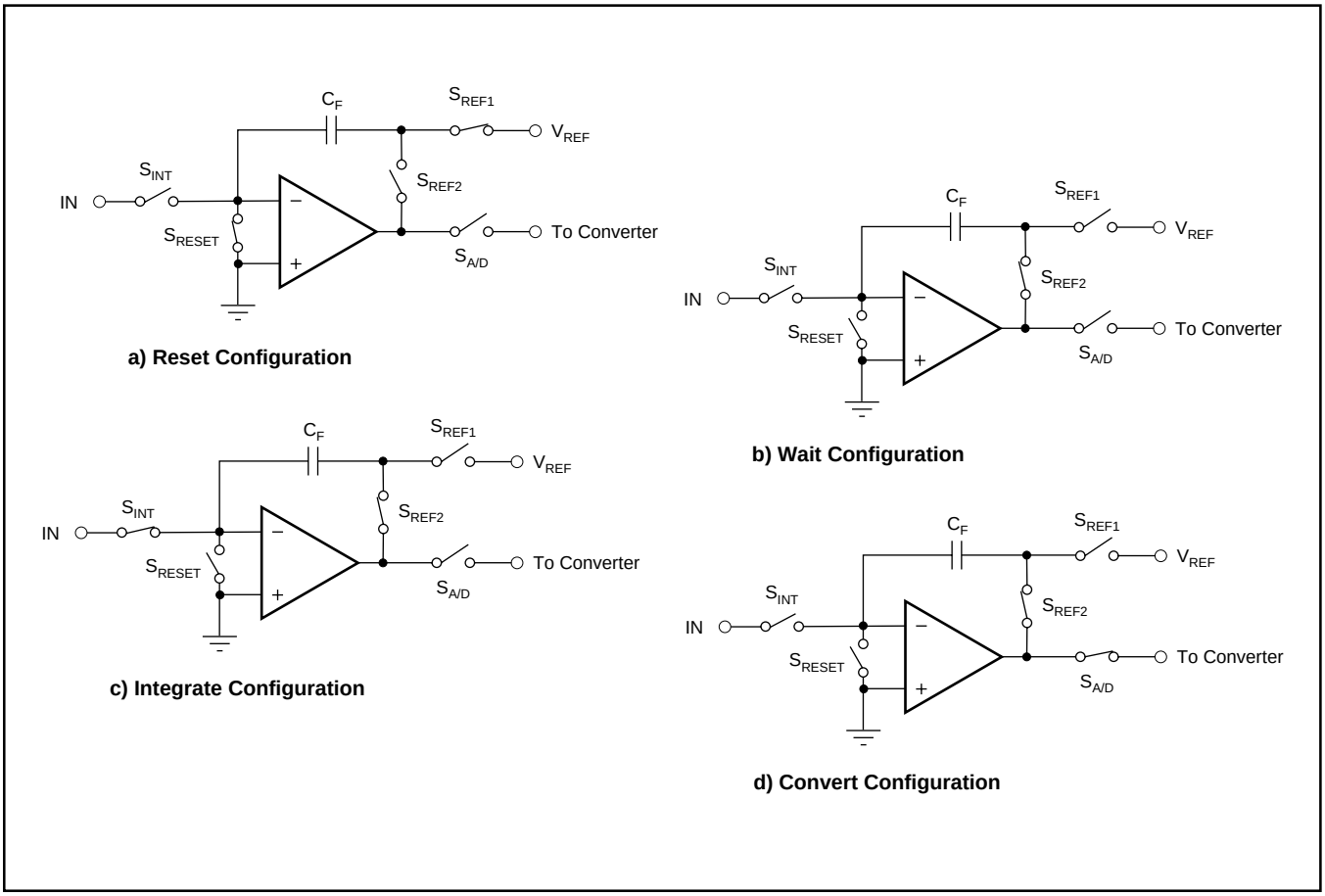


FIGURE 5. Diagrams for the Four Configurations of the Front End Integrators of the DDC112.

Determining the Integration Capacitor (C_F) Value

The value of the integrator's feedback capacitor, the integration period, and the reference voltage determine the positive full-scale (+FS) value of the DDC112 . The approximate positive full-scale value of the DDC112 is given by the following equations:

$$Q_{IN} = I_{IN} \bullet T_{INT}$$

$$Q_{FS} \approx (0.96)\, V_{REF} \bullet C_F$$

$$I_{FS} \approx \frac{(0.96)\, V_{REF} \bullet C_F}{T_{INT}}$$

or

$$C_F \approx \frac{I_{FS} \bullet T_{INT}}{(0.96)\, V_{REF}}$$

The negative full-scale (–FS) range is approximately 0.4% of the positive full-scale range. For example, Range 5 has a nominal +FS range of 250pC. The –FS range is then approximately –1pC. This relationship holds for external capacitors as well and is independent of V_{REF} (for V_{REF} within the allowable range, see the Specification table).

Integration Capacitors

There are seven different capacitors available on chip for each side of each channel in the DDC112. These internal capacitors are trimmed in production to achieve the specified performance for range error of the DDC112. The range control pins (RANGE0-RANGE2) change the capacitor value for all four integrators. Consequently, both inputs and both sides of each input will always have the same full scale range unless external capacitors are used.

External integration capacitors may be used instead of the internal capacitors values by setting RANGE2-RANGE0 = 000. The external capacitor pin connections are summarized in Table II. Usually, all four external capacitors are equal in value, however, it is possible to have differing pairs of external capacitors between Input 1 and Input 2 of the DDC112. Regardless of the selected value of the capacitor, it is strongly recommended that the capacitors for sides A and B be the same.

EXTERNAL CAPACITOR PINS ON THE DDC112	INTEGRATOR	
	Channel	Side
5 and 6	1	A
3 and 4	1	B
23 and 24	2	A
25 and 26	2	B

TABLE II. External Capacitor Connections with Range Configuration of RANGE2-RANGE0 = 000.

Since the range accuracy depends on the characteristics of the integration capacitor, they must be carefully selected. An external integration capacitor should have low voltage coefficient, temperature coefficient, memory, and leakage current. The optimum selection depends on the requirements of the specific application. Suitable types include COG ceramic, polycarbonate, polystyrene, and silver mica.

Voltage Reference

The external voltage reference is used to reset the integration capacitors before an integration cycle begins. It is also used by the ΔΣ converter while the converter is measuring the voltage stored on the integrators after an integration cycle ends. During this sampling, the external reference must supply charge needed by the ΔΣ converter. For an integration time of 500µs, this charge translates to an average V_{REF} current of approximately 150µA. The amount of charge needed by the ΔΣ converter is independent of the integration time, therefore, increasing the integration time lowers the average current. For example, an integration time of 1000µs lowers to average V_{REF} current to 75µA.

It is critical that V_{REF} be stable during the different modes of operation shown in Figure 5. The ΔΣ converter measures the voltage on the integrator with respect to V_{REF}. Since the integrator's capacitors are initially reset to V_{REF}, any droop in V_{REF} from the time the capacitors are reset to the time when the converter measures the integrator's output will introduce an offset. It is also important that V_{REF} be stable over longer periods of time as changes in V_{REF} correspond directly to changes in the full-scale range. Finally, V_{REF} should introduce as little additional noise as possible.

For reasons mentioned above, it is strongly recommended that the external reference source be buffered with an operational amplifier as shown in Figure 6. In this circuit, the voltage reference is generated by a 4.096V reference. A

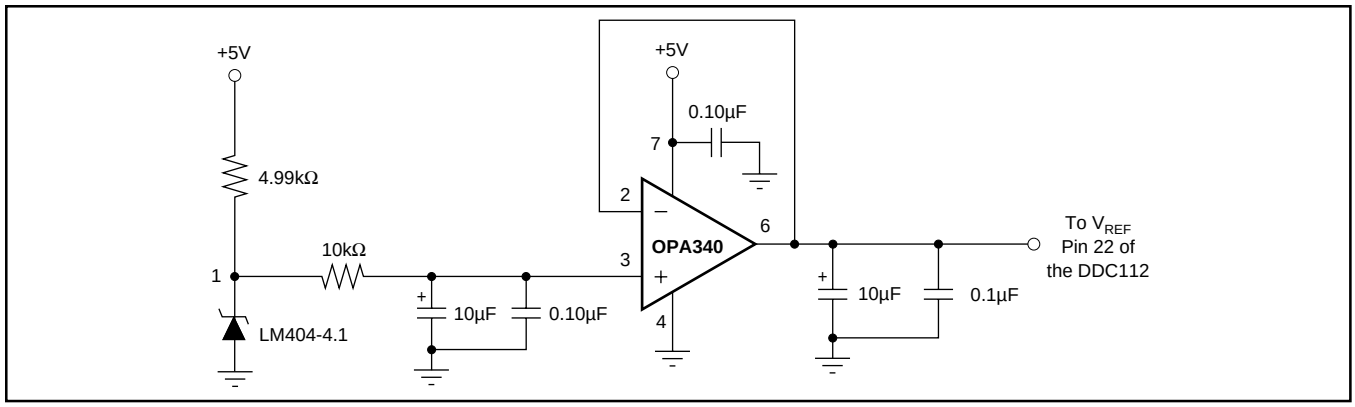


FIGURE 6. Recommended External Voltage Reference Circuit for Best Low Noise Operation with the DDC112.

low-pass filter to reduce noise connects it to an operational amplifier configured as a buffer. This amplifier should have a unity gain bandwidth greater than 4MHz, low noise, and input/output common-mode ranges that support V_{REF}. Following the buffer are capacitors placed close to the DDC112's V_{REF} pin. Even though the circuit in Figure 6 might appear to be unstable due to the large output capacitors, it works well for most operational amplifiers. It is NOT recommended that series resistance be placed in the output lead to improve stability since this can cause droop in V_{REF} which produces large offsets.

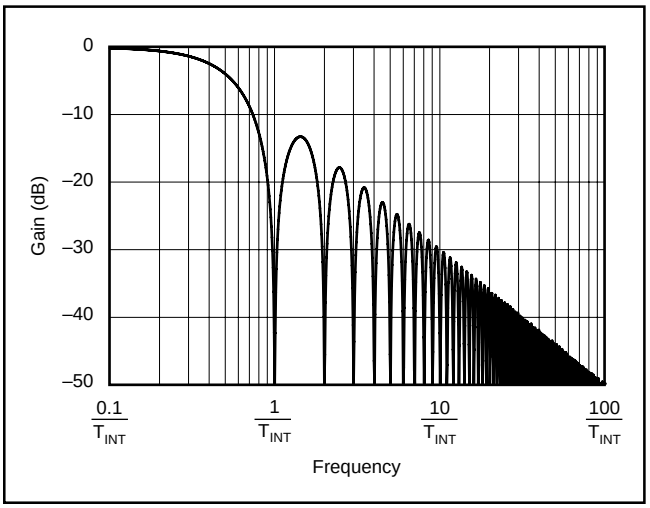


FIGURE 7. Frequency Response of the DDC112.

DDC112 Frequency Response

The frequency response of the DDC112 is set by the front end integrators and is that of a traditional continuous time integrator (see Figure 7). By adjusting T_{INT}, the user can change the 3dB bandwidth and the location of the notches in the response. The frequency response of the ΔΣ converter that follows the front end integrator is of no consequence because the converter samples a held signal from the integrators. That is, the input to the ΔΣ converter is always a DC signal. Since the output of the front end integrators are sampled, aliasing can occur. Whenever the frequency of the input signal exceeds one-half of the sampling rate, the signal will "fold" back down to lower frequencies.

Test Mode

When TEST is used, pins IN1 and IN2 are grounded and "packets" of approximately 13pC charge are transferred to the integration capacitors of both Input 1 and Input 2. This fixed charge can be transferred to the integration capacitors either once during an integration cycle or multiple times. In the case where multiple packets are transferred during one integration period, the 13pC charge is additive. This mode can be used in both the continuous and non-continuous mode timing. The timing diagrams for test mode are shown in Figure 8. The top three lines in Figure 8 define the timing when one packet of 13pC is sent to the integration capacitors. The bottom three lines define the timing when multiple packets are sent to the integration capacitors.

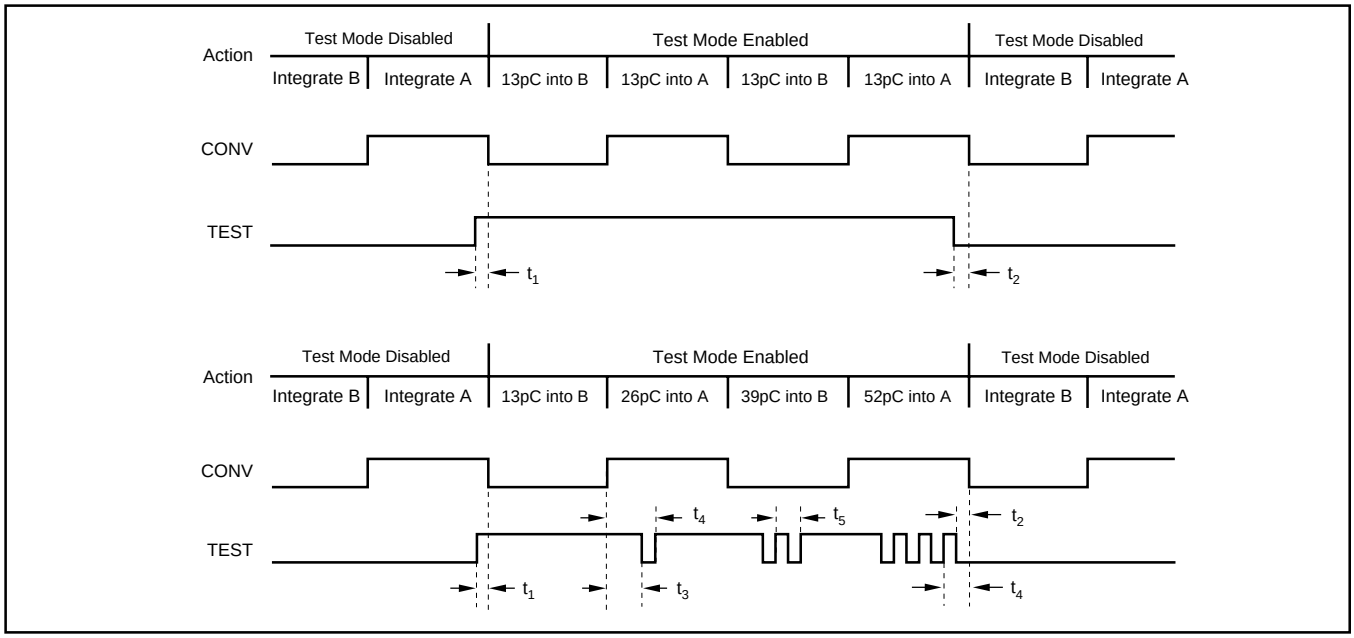


FIGURE 8. Timing Diagram of the Test Mode of the DDC112.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Setup Time for Test Mode Enable	100			ns
t_2	Setup Time for Test Mode Disable	100			ns
t_3	Hold Time for Test Mode Enable	100			ns
t_4	From Rising edge of TEST to the Edge of CONV while Test Mode Enabled	5.4			µs
t_5	Rising Edge to Rising Edge of TEST	5.4			µs

TABLE III. Timing for the DDC112 in the Test Mode, CLK = 10MHz.

TEST and CONV work together to implement this feature. The test mode is entered when TEST is HIGH prior to a CONV edge. At that point, a CONV edge triggers the grounding of the analog inputs and the switching of 13pC packets of charge onto the integration capacitors. If TEST is kept HIGH through at least two conversions (i.e., a rise and fall of CONV), all four integrators will be charged with a 13pC packet. At the end of each conversion, the voltage at the output of the integrators is digitized as discussed in the "Continuous Mode" and "Non-Continuous Mode" section of this data sheet. The test mode is exited when TEST is LOW and a CONV edge occurs.

Once the test mode is entered as described above, TEST can cycle as many times as desired. When this is done, additional 13pC packets are added on the rising edge of TEST to the existing charge on the integrator capacitors. Multiple charge packets can be added in this way as long as the TEST pin is not LOW when CONV toggles.

DIGITAL ISSUES

The digital interface of the DDC112 provides the digital results via a synchronous serial interface consisting of a data clock (DCLK), a transmit enable pin (DXMIT), a valid data pin (DVALID), a serial data output pin (DOUT), and a serial data input pin (DIN). The DDC112 contains only one A/D converter, so the conversion process is interleaved between the two inputs as shown in Figure 2. The integration and conversion process is fundamentally independent of the data retrieval process. Consequently, the CLK frequency and DCLK frequencies need not be the same. DIN is used when multiple converters are cascaded. Cascading or "daisy chaining" greatly simplifies the interconnection and routing of the digital outputs in cases where a large number of converters are needed. Refer to "Cascading Multiple Converters" section of this data sheet for more detail.

The conversion rate of the DDC112 is set by a combination of the integration time (determined by the user) and the speed of the A/D conversion process. The A/D conversion time is primarily a function of the system clock (CLK) speed. One A/D conversion cycle encompasses the conversion of two signals (one from each input of the DDC112) and reset time for each of the integrators involved in the two conversions. In most situations, the A/D conversion time is shorter than the integration time. If this condition exists, the DDC112 will operate in the continuous mode. When the DDC112 is in the continuous mode, the sensor output is continuously integrated by one of the two sides of each input.

In the event that the A/D conversion takes longer than the integration time, the DDC112 will switch into a non-continuous mode. In non-continuous mode, the A/D converter is not able to keep pace with the speed of the integration process. Consequently, the integration process is periodically halted until the digitizing process catches up. These two basic modes of operation for the DDC112—continuous and non-continuous modes—are described below.

Continuous Mode

As shown in Figure 9, CONV controls which side is integrating the input signal. When CONV toggles, one side will stop integrating while the other side begins. Side A is integrating when CONV is HIGH, conversely, side B is integrating when CONV is LOW. CONV also controls the measurement of the integrators by the A/D converter. Once a side is finished integrating, it must be measured then reset so it can integrate again when the other side completes its integration. Input 1's integrator is measured first, followed by Input 2. When they are done, the integrators are reset and then wait until a new integration cycle begins. The data becomes available when both integrators have been measured. This is indicated by $\overline{\text{DVALID}}$ going LOW. This signal stays LOW until $\overline{\text{DXMIT}}$ is taken LOW and the data is retrieved.

Non-Continuous Mode

For certain applications, it is desirable to be able to set the integration time to be shorter than that required to completely measure and reset the integrators. For these integration times, the DDC112 enters the non-continuous mode. In this mode, the charge is only integrated a fraction of the total time. Once the measurements are complete and the sides reset, integration can begin again. As with the continuous mode, CONV determines the status of the integrations and is used to control overall operation.

Figure 10 illustrates an example of operation in the non-continuous mode. As can be seen in Figure 10, the integration on side B is terminated before the A/D conversion process is finished on the side A integrators. The side A integrators are not ready to begin another integration cycle and the DDC112 enters a "wait" state while the conversion process is completed. First, the side A integrators are finished being measured and then side B integrators are measured. Afterwards, the integrators are reset to prepare them for integrating again. When the wait state is completed, the DDC112 passes through a "release" state when CONV toggles. Upon the next transition of CONV, the integration cycle begins again as the entire cycle repeats.

The data readback behaves the same in the non-continuous mode as it does in the continuous mode. When side A's data is ready, $\overline{\text{DVALID}}$ goes LOW. Then, when side B's data is ready, $\overline{\text{DVALID}}$ goes LOW again. The readback of side A's data must be completed before side B's data is ready. This prevents the side B data from writing over the results from side A since a single internal shift register is used for readback.

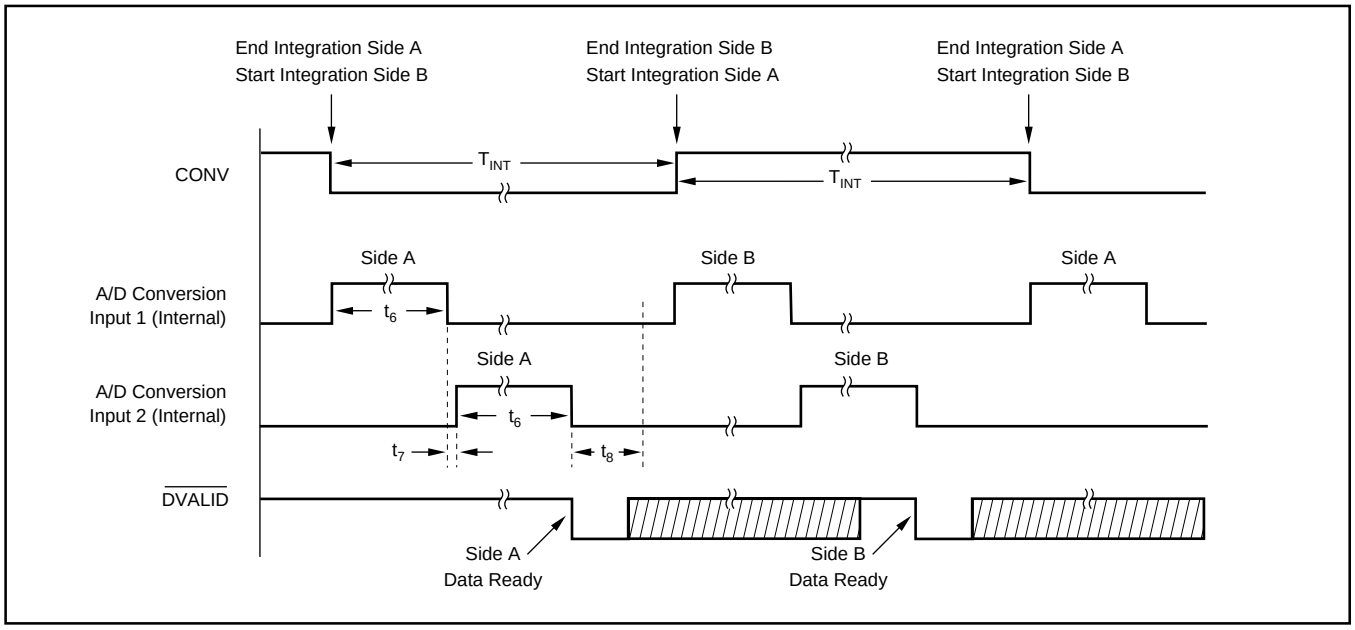


FIGURE 9. Timing Diagram of the Continuous Mode of the DDC112.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
T_{INT}	Integration Period (continuous mode)	500		1,000,000	µs
t_6	A/D Conversion Time (internally controlled)		202.2		µs
t_7	A/D Conversion Reset Time (internally controlled)		13.2		µs
t_8	Integrator and A/D conversion Reset Time (internally controlled)		61.8		µs

TABLE IV. Timing for the DDC112 in the Continuous Mode, CLK = 10MHz.

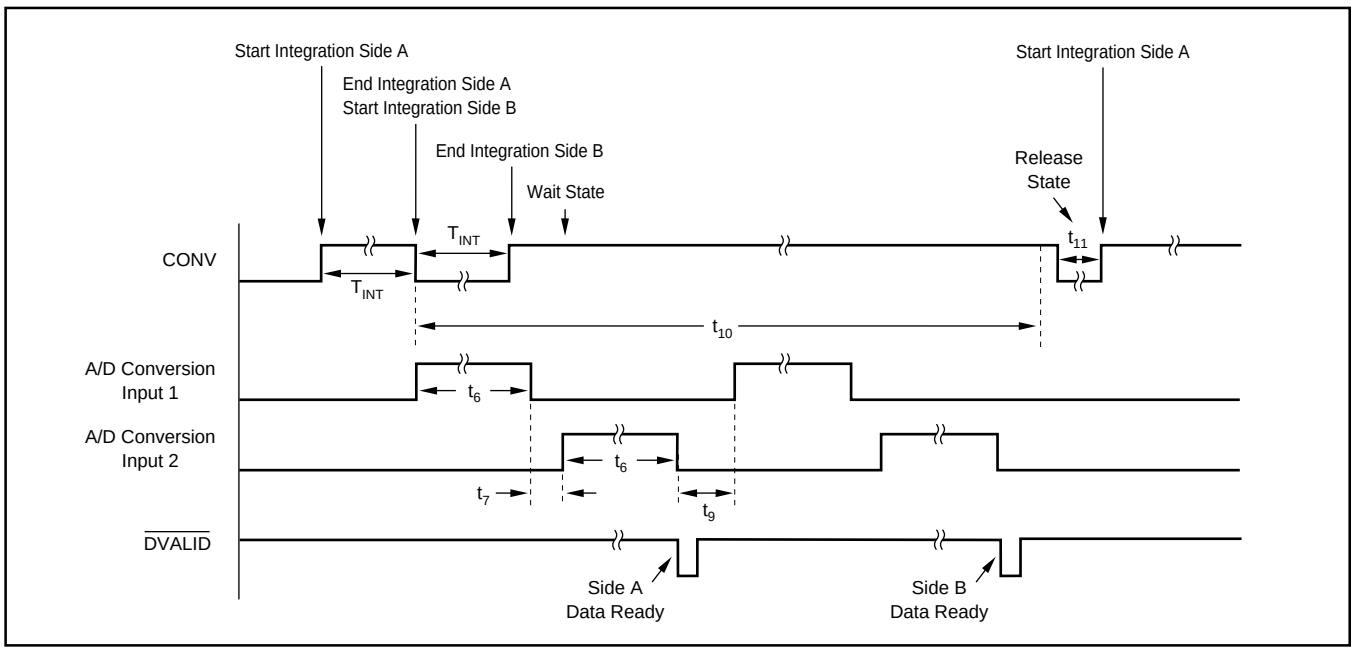


FIGURE 10. Timing Diagram of the Non-Continuous Mode with Side A Integrated First.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
T_{INT}	Integration Time (non-continuous mode)	50			µs
t_6	A/D Conversion Time (internally controlled)		202.2		µs
t_7	A/D Conversion Reset Time (internally controlled)		13.2		µs
t_9	Integration and A/D Conversion Reset Time (internally controlled)		37.8		µs
t_{10}	Total A/D Conversion and Reset Time (internally controlled)		910.8		µs
t_{11}	Release Time	24			µs

TABLE V. Timing for the DDC112 in the Non-Continuous Mode, CLK = 10MHz.

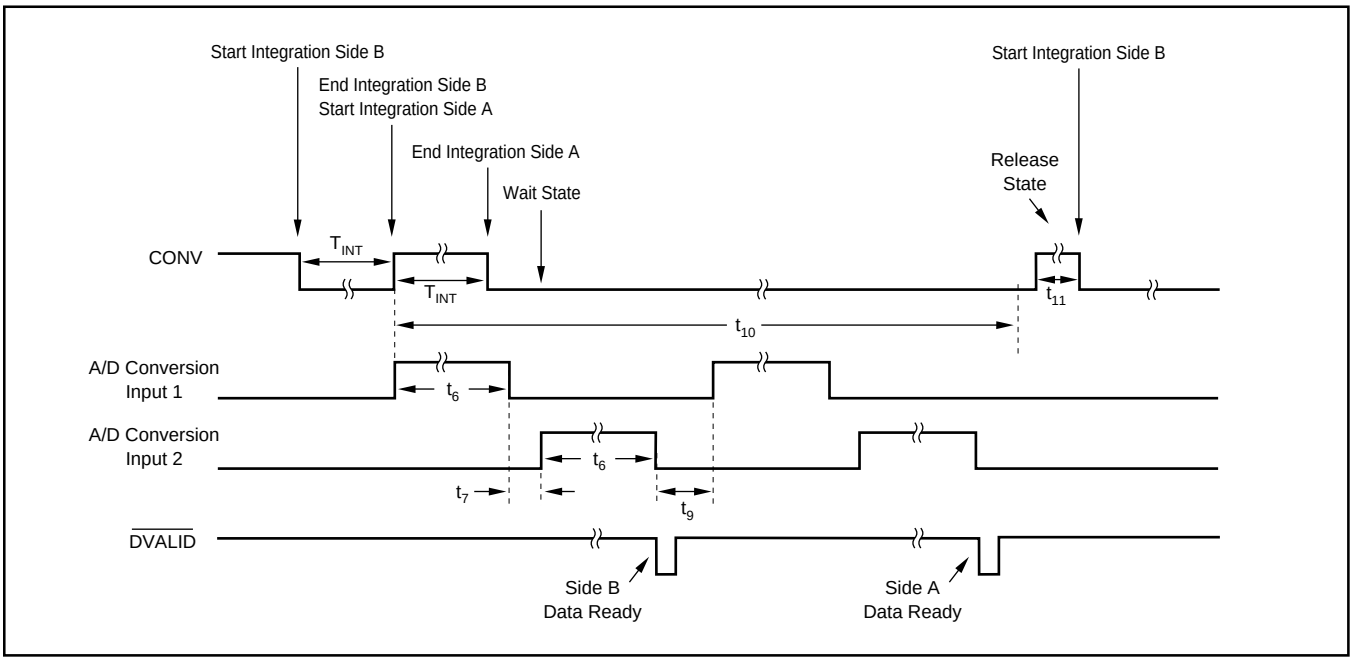
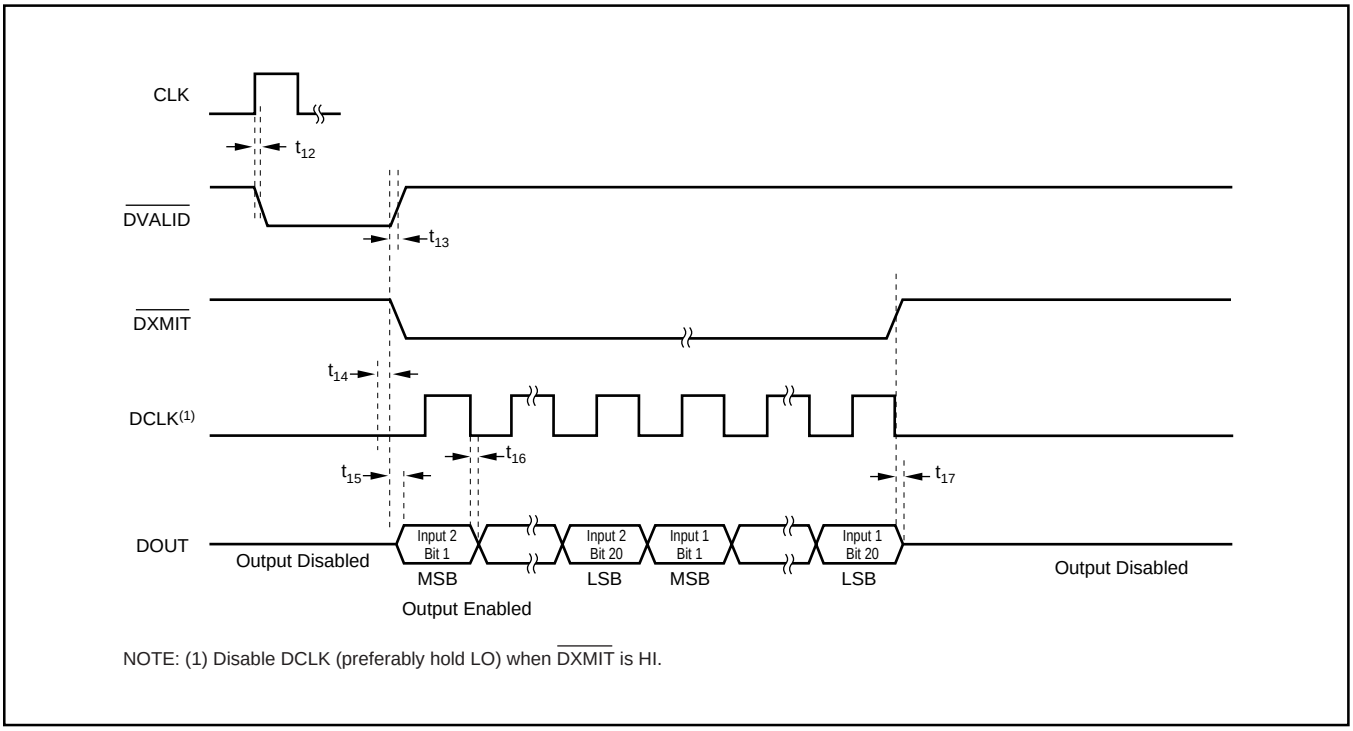


FIGURE 11. Timing Diagram of the Non-Continuous Mode with Side B of Both Integrated First.



NOTE: (1) Disable DCLK (preferably hold LO) when $\overline{DXMIT}$ is HI.

FIGURE 12. Digital Interface Timing Diagram for Data Retrieval From a Single DDC112.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{12}	Propagation Delay from Rising Edge of CLK to $\overline{DVALID}$ LOW	30			ns
t_{13}	Propagation Delay from $\overline{DXMIT}$ LOW to $\overline{DVALID}$ HIGH	30			ns
t_{14}	Setup Time from DCLK LOW TO $\overline{DXMIT}$ LOW		20		ns
t_{15}	Propagation Delay from $\overline{DXMIT}$ LOW to Valid DOUT			30	ns
t_{16}	Hold Time that DOUT is Valid After Falling Edge of DCLK	5			ns
t_{17}	Propagation Delay from $\overline{DXMIT}$ HIGH to DOUT Disabled		30		ns

TABLE VI. Timing for the DDC112 Data Retrieval.

It is possible to change the CONV pattern so that side B integrates before side A. This is shown in Figure 11. In either case and also for the continuous mode, the integrations always alternate between sides A and B. That is, that data output is always of the form A, B, A, B, A, B, etc.

In the non-continuous mode, the input signal is not being integrated. To prevent the input signal from charging up the input of the DDC112 during this time, the DDC112 shorts its inputs to ground when it is not integrating. When an integration begins, the switches are opened and the input signal is re-routed to the integrators.

Data Retrieval

In the continuous and non-continuous modes of operation, the data from the last conversion is available for retrieval with the falling edge of $\overline{\text{DVALID}}$ (see Figure 12). The falling edge of DXMIT in combination with the data clock (DCLK) will initiate the serial transmission of the data from the DDC112. Typically, data is retrieved from the DDC112 as soon as $\overline{\text{DVALID}}$ falls and completed before the next CONV transition from HIGH to LOW or LOW to HIGH occurs. If this is not the case, care should be taken to stop activity on DCLK and consequently DOUT by at least 10µs around a CONV transition. If this caution is ignored it is possible that the integration that is being initiated by CONV will have additional noise introduced.

The serial output data at DOUT is transmitted in Straight Binary Code per Table VII. An output offset has been built into the DDC112 to allow for the measurement of input signals near and below zero. Board leakage up to ≈ –0.4% of the positive full scale can be tolerated before the digital output clips to all zeroes.

CODE	INPUT SIGNAL
1111 1111 1111 1111 1111	FS
1111 1111 1111 1111 1110	FS – 1LSB
0000 0001 0000 0000 0001	+1LSB
0000 0001 0000 0000 0000	Zero
0000 0000 0000 0000 0000	–0.4% FS

TABLE VII. Straight Binary Code Table.

Cascading Multiple Converters

Multiple DDC112 units can be connected in serial or parallel configurations, as illustrated in Figures 13 and 14.

DOUT can be used with DIN to "daisy chain" several DDC112 devices together to minimize wiring. In this mode of operation, the serial data output is shifted through multiple DDC112s, as illustrated in Figure 13.

R_{PULLUP} prevents DIN from floating when $\overline{\text{DXMIT}}$ is HI.

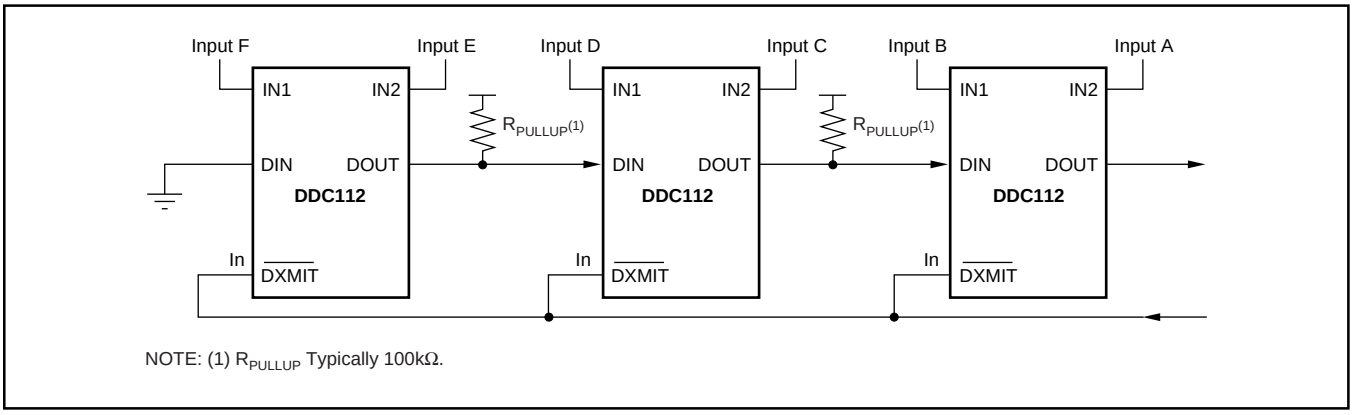


FIGURE 13. Daisy-Chained DDC112's.

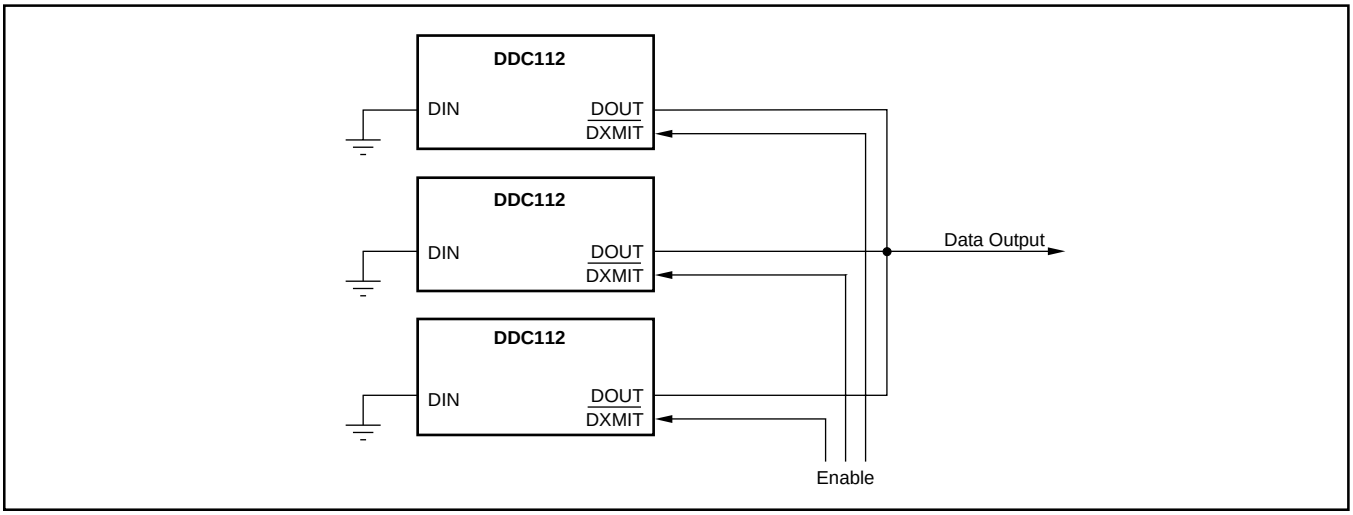
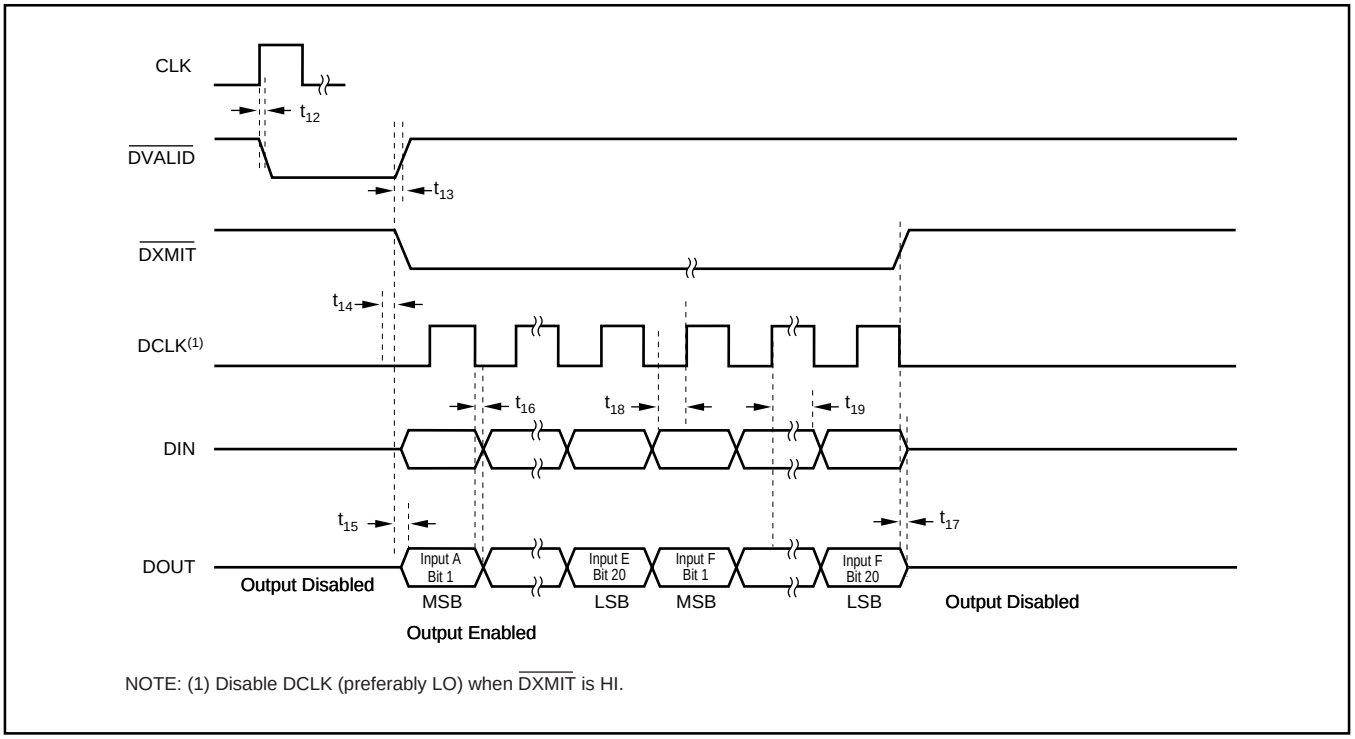


FIGURE 14. DDC112 in Parallel Operation.



NOTE: (1) Disable DCLK (preferably LO) when $\overline{DXMIT}$ is HI.

FIGURE 15. Timing Diagram When Using the DIN Function of the DDC112.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{18}	Set-Up Time From DIN to Rising Edge of DCLK	10			ns
t_{19}	Hold Time For DIN After Rising Edge of DCLK	10			ns

TABLE VIII. Timing for the DDC112 Data Retrieval Using DIN.

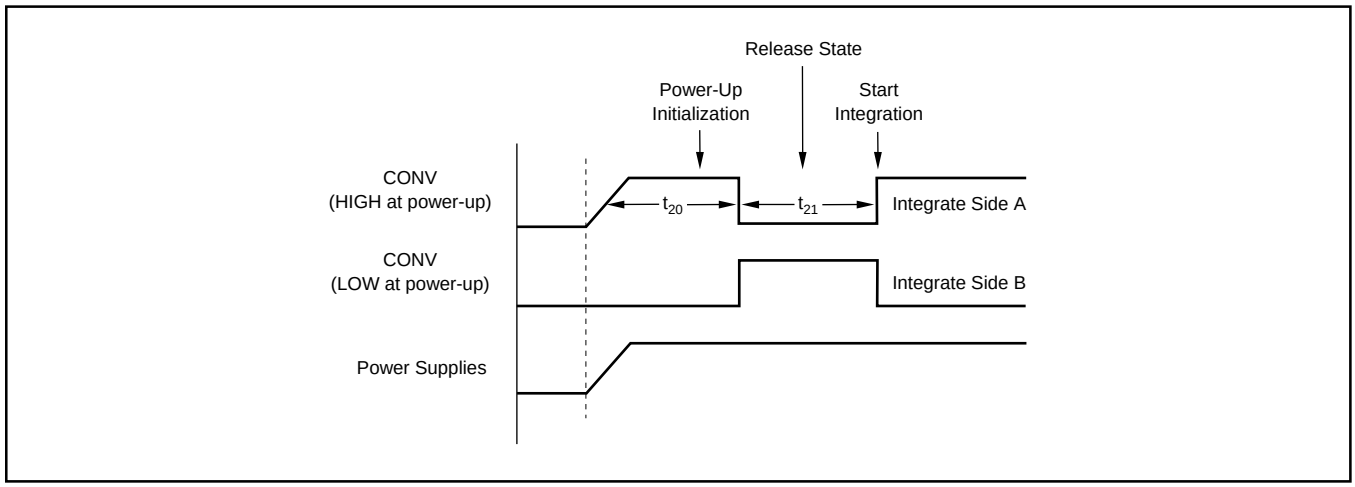


FIGURE 16. Timing Diagram at Power-Up of the DDC112.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{20}	Power-On Initialization Period	50			µs
t_{21}	From Release Edge to Integration Start	50			µs

TABLE IX. Timing for the DDC112 Power-Up Sequence.

POWER-UP SEQUENCING

Prior to power-up, all digital and analog input pins must be LOW. At the time of power-up, these signal inputs can be biased to a voltage other than 0V, however, they should never exceed AV_{DD} or DV_{DD}. The level of CONV at power-up is used to determine which side (A or B) will be integrated first. Before integrations can begin though, CONV must toggle as shown in Figure 16.

LAYOUT

Power Supplies and Grounding

Both AV_{DD} and DV_{DD} should be as quiet as possible. It is particularly important to eliminate noise from AV_{DD} that is non-synchronous with the DDC112 operation. Figure 17 illustrates two acceptable ways to supply power to the DDC112. The first case shows two separate +5V supplies for AV_{DD} and DV_{DD}. In this case, each +5V supply of the DDC112 should be bypassed with 10µF solid tantalum capacitors and 0.1µF ceramic capacitors. The second case shows the DV_{DD} power supply derived from the AV_{DD} supply with a < 10Ω isolation resistor. In both cases, the 0.1µF capacitors should be placed as close to the DDC112 package as possible.

Shielding Analog Signal Paths

As with any precision circuit, careful printed circuit layout will ensure the best performance. It is essential to make short, direct interconnections and avoid stray wiring capacitance—particularly at the analog input pins. Digital signals should be kept as far from the analog input signals as possible on the PC board.

Input shielding practices should be taken into consideration when designing the circuit layout for the DDC112. The inputs to the DDC112 are high impedance and extremely sensitive to extraneous noise. Leakage currents between the PCB traces can exceed the input bias current of the DDC112 if shielding is not implemented. Figure 18 illustrates an acceptable approach to this problem. In this diagram, a PC trace shield is placed around the input pins. When using external integration capacitors, place guard lines around pins 3, 5, 24, and 26 as these connect internally to the input integrator.

The shield pattern reduces leakage affects by surrounding these sensitive pins with a low impedance analog ground. Leakage currents from other portions of the circuit will flow harmlessly to the low impedance analog ground rather than into the analog input stage of the DDC112. Analog ground pins are placed next to the analog input pins in the DDC112 package to allow convenient layout of this shield.

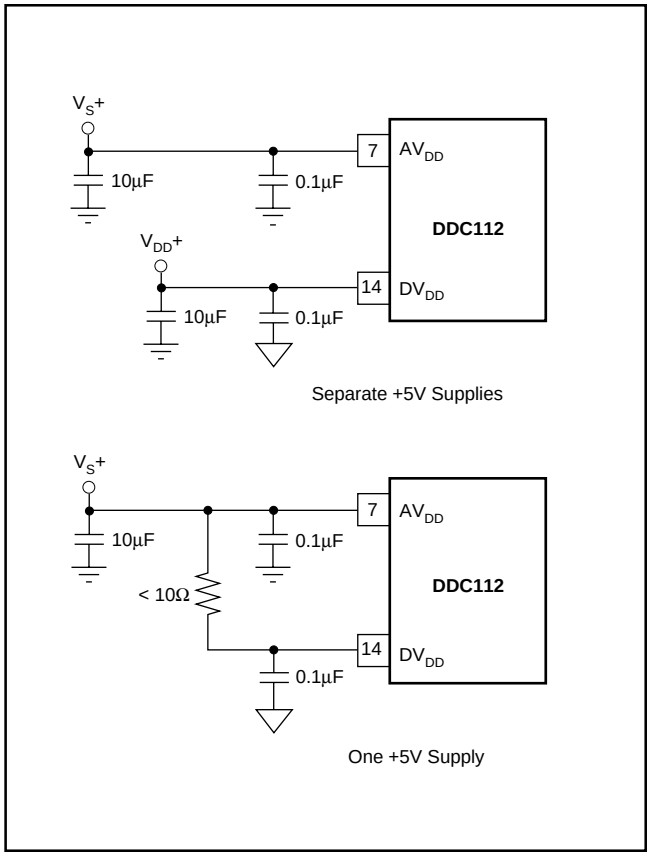


FIGURE 17. Power Supply Connection Options.

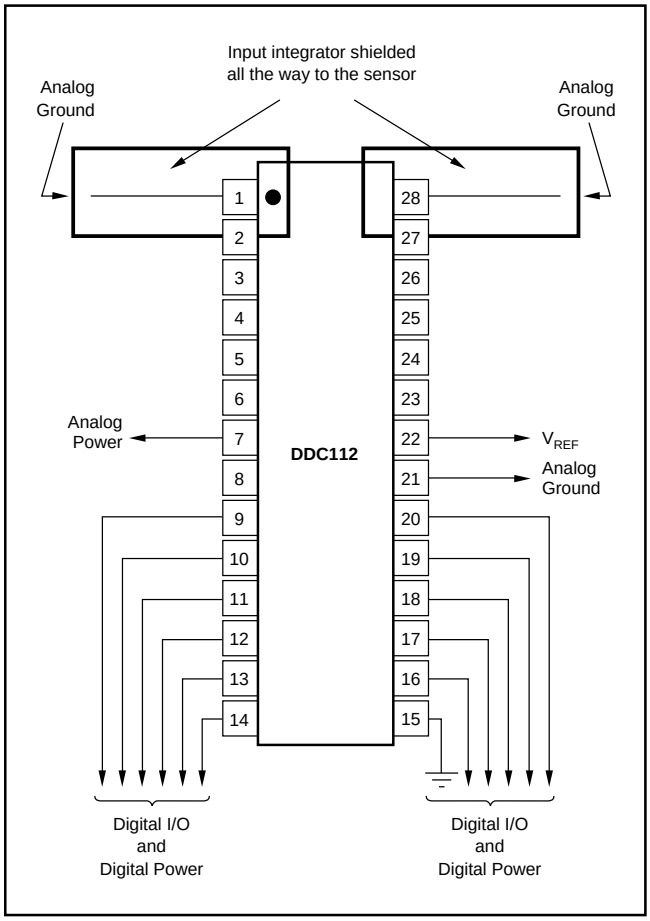


FIGURE 18. Recommended Shield for DDC112 Layout Design.